ELECTRONICS

Assignment 1

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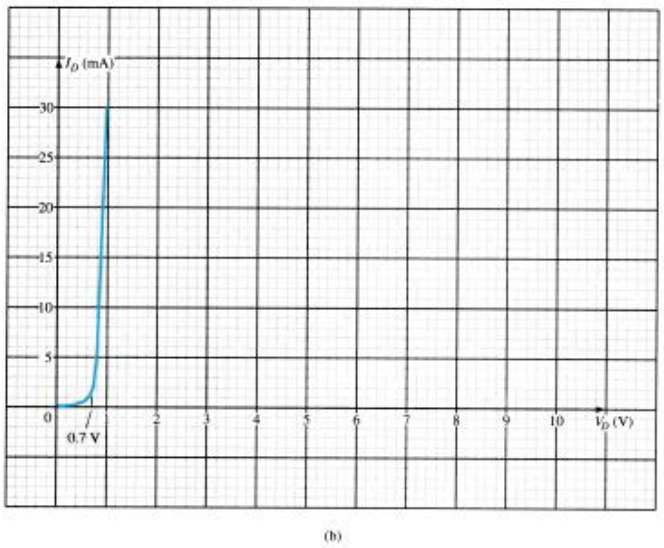
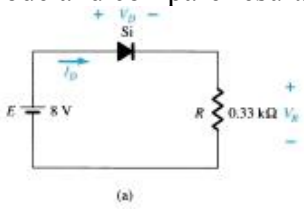
Section:2918

43908974

1. (a) Using the characteristics of Fig. 2.131b, determine ID, VD, and VR for the circuit of Fig. 2.131a.
(b) Repeat part (a) using the approximate model for the diode and compare results.
(c) Repeat part (a) using the ideal model for the diode and compare results.



(b)



(a)

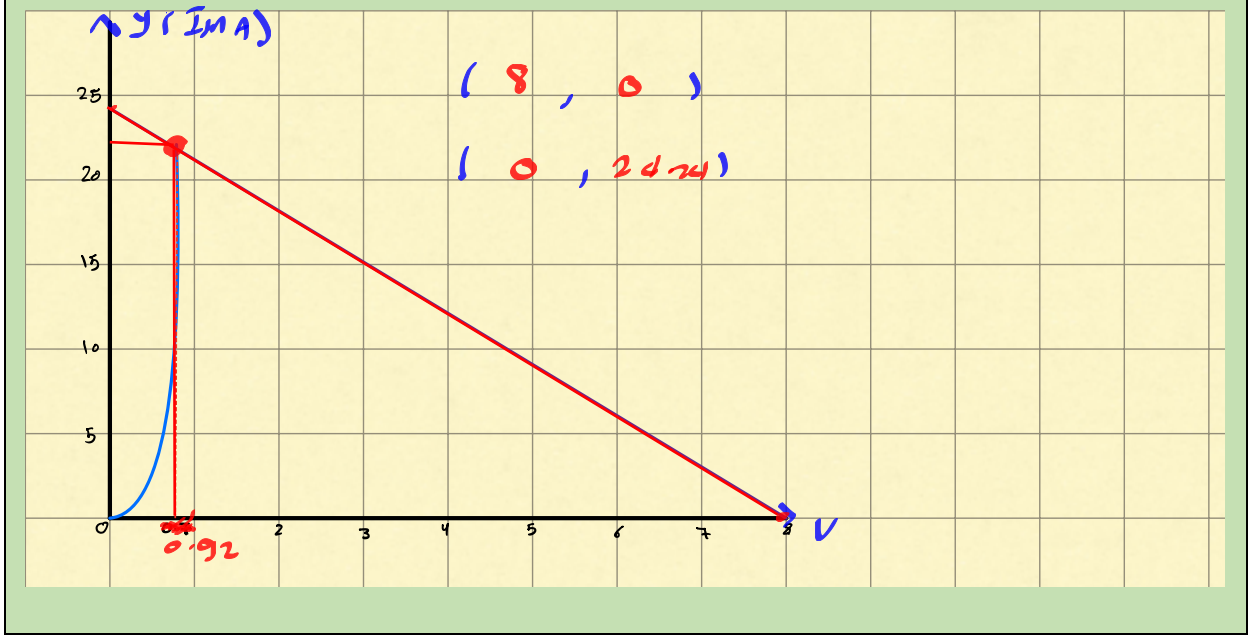
(a) Using the characteristics of Fig. 2.131b, determine ID, VD, and VR for the circuit of Fig. 2.131a.

Note ID =E/R=8/0.33K=24.24 mA, VD = E = 8 V

$E = V_D + I_D R$

$I_D = \frac{E}{R}$

$I_{DQ} = 21$ mA
$V_{DQ} = 0.92$ V
$V_R = E - V_{DQ} = 8 - 0.92 = 7.08$ V

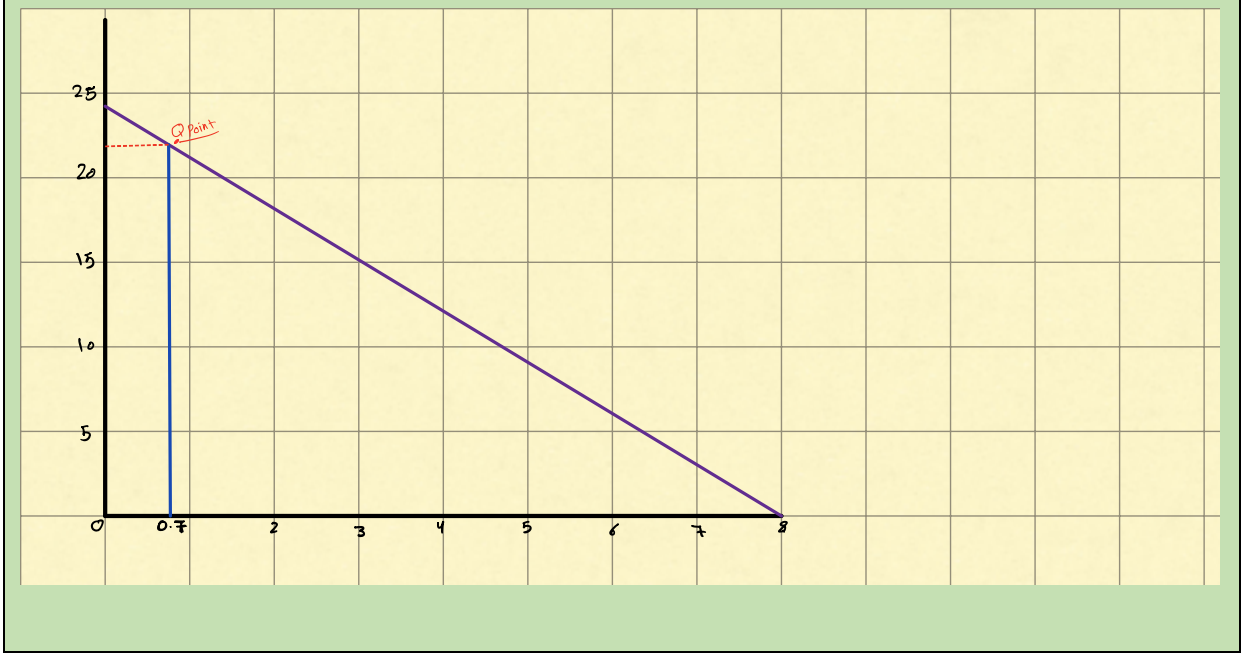


(b) Repeat part (a) using the approximate model for the diode and compare results.

$I_{DQ} = 22$ mA

$V_{DQ} = 0.7$ V

$V_R = E - V_{DQ} = 8 - 0.7 = 7.3$ V

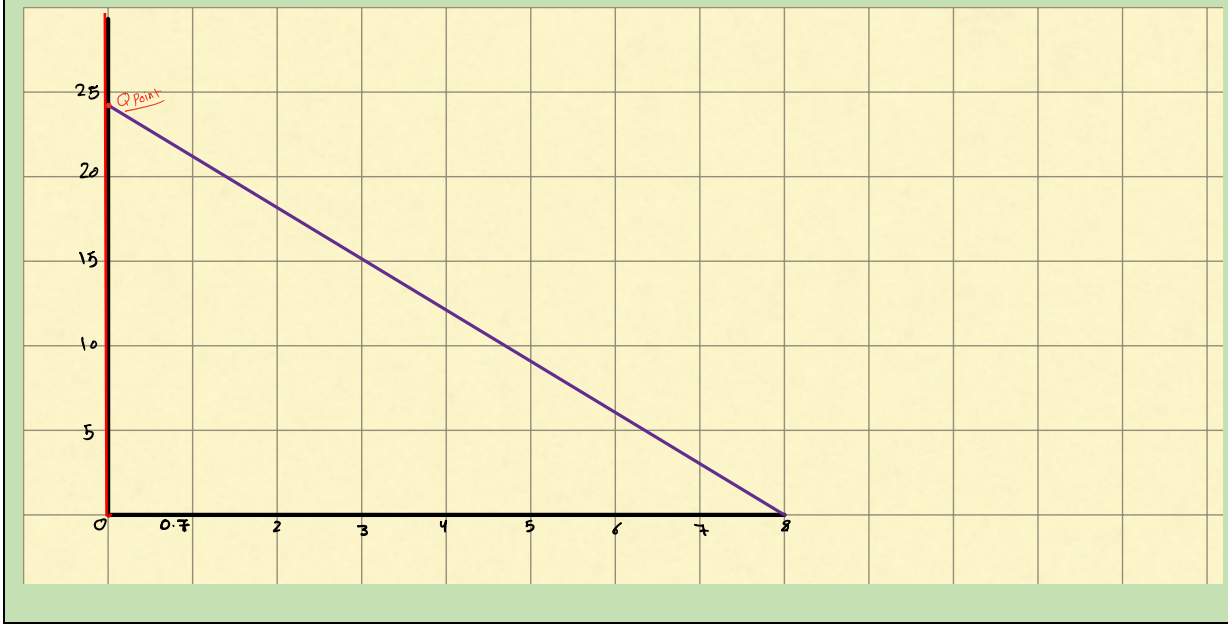


(c) Repeat part (a) using the ideal model for the diode and compare results.

$I_{DQ} = 24.24$ mA

$V_{DQ} = 0$ V

$V_R = E - V_{DQ} = 8 - 0 = 8$ V



2. (a) Using the characteristics of Fig. 2.131b, determine *ID* and *VD* for the circuit of Fig. 2.132.
(b) Repeat part (a) with $R = 0.47\ k\Omega$.
(c) Repeat part (a) with $R = 0.18\ k\Omega$.
(d) Is the level of *VD* relatively close to 0.7 V in each case?
How do the resulting levels of *ID* compare? Comment accordingly.

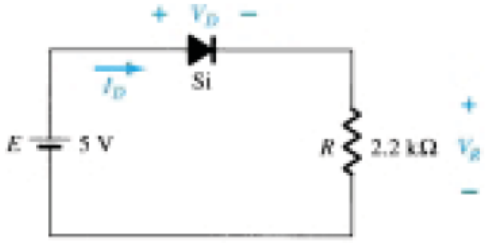
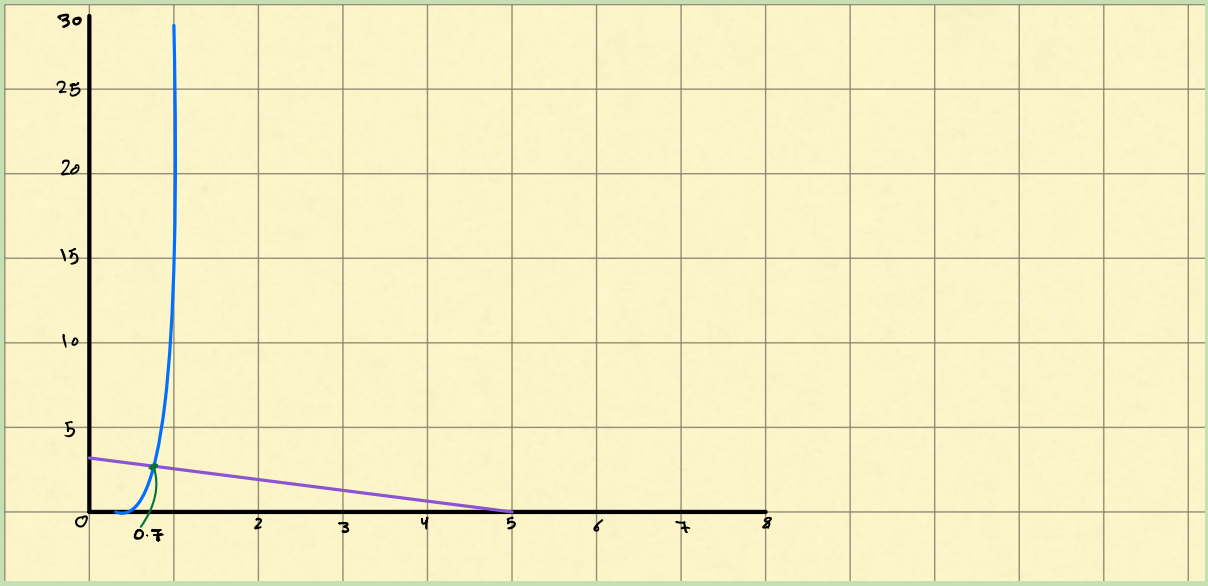


Figure 2.132 Problems 2, 3

(a) Using the characteristics of Fig. 2.131b, determine *ID* and *VD* for the circuit of Fig. 2.132.

$$I_D = \frac{E}{R} = \frac{5}{2.2K} = 2.27\ mA \text{ - } V_D = 5\ V$$

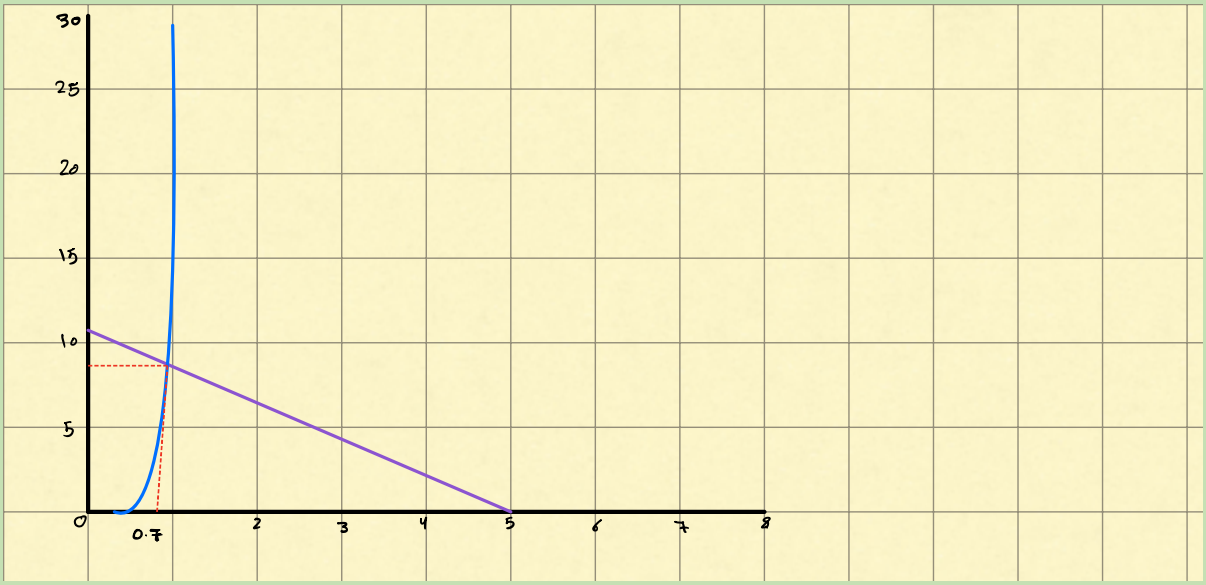
$$I_{DQ} = 2\ mA \text{ - } V_{DQ} = 0.7\ V$$



(b) Repeat part (a) with $R = 0.47\ k\Omega$.

$$I_D = \frac{E}{R} = \frac{5}{0.47K} = 10.64\ mA - V_D = 5\ V$$

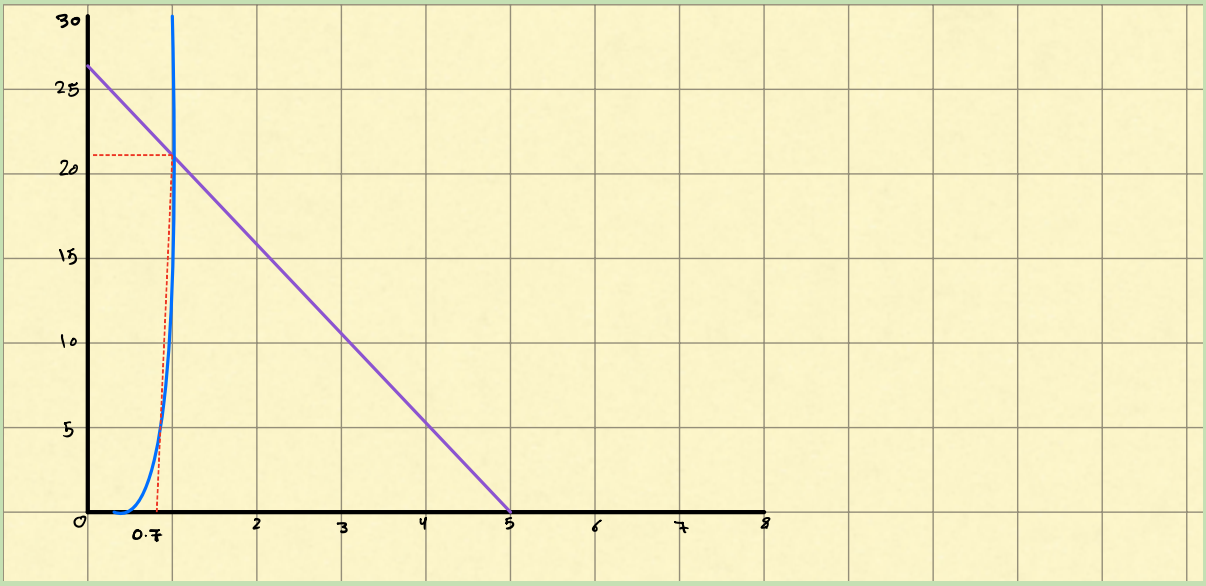
$$I_{DQ} = 9\ mA - V_{DQ} = 0.8\ V$$



(c) Repeat part (a) with $R = 0.18\ k\Omega$.

$$I_D = \frac{E}{R} = \frac{5}{0.18K} = 27.78\ mA - V_D = 5\ V$$

$$I_{DQ} = 22.5\ mA - V_{DQ} = 0.93\ V$$

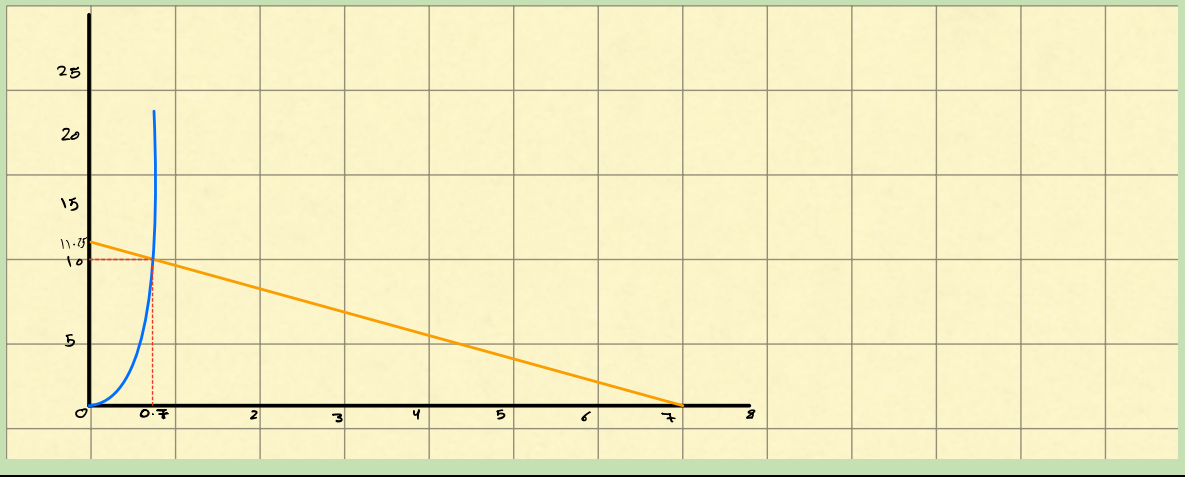


3. Determine the value of R for the circuit of Fig. 2.132 that will result in a diode current of 10 mA if E = 7 V. Use the characteristics of Fig. 2.131b for the diode.

Note $V_D = 7\ V - I_{DQ} = 10\ mA$

$I_D = 11.25\ mA$

$$R = \frac{7\ V}{11.25\ mA} = 0.62\ k\Omega$$



4. (a) Using the approximate characteristics for the Si diode, determine the level of VD, ID, and VR for the circuit of Fig. 2.133.
(b) Perform the same analysis as part (a) using the ideal model for the diode.
(c) Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

Figure 2.133 Problem 4

(a) Using the approximate characteristics for the Si diode, determine the level of VD, ID, and VR for the circuit of Fig. 2.133.

$V_R = E - V_D = 30 - 0.7 = 29.3\ V\ \&\ V_D = 0.7\ V$

$$I_D = \frac{V_R}{R} = \frac{29.3}{2.2K} = 13.32\ mA$$

(b) Perform the same analysis as part (a) using the ideal model for the diode.

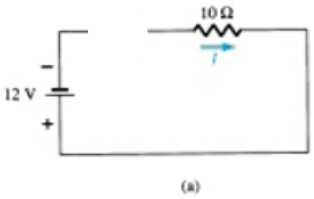
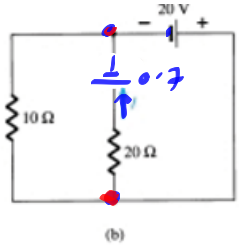
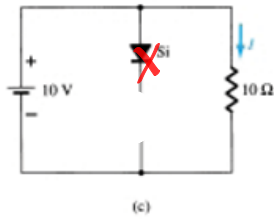
$V_R = E - V_D = 30 - 0 = 30\ V\ \&\ V_D = 0\ V$

$$I_D = \frac{V_R}{R} = \frac{30-0}{2.2K} = 13.64\ mA$$

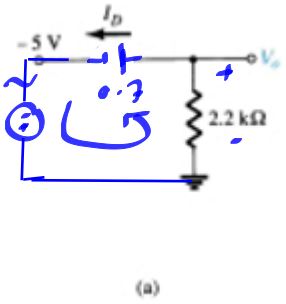
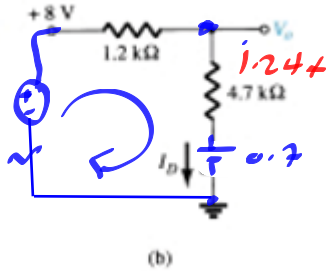
(c) Do the results obtained in parts (a) and (b) suggest that the ideal model can provide a good approximation for the actual response under some conditions?

Yes, since E>> Vt levels of I_D and V_D are quite close

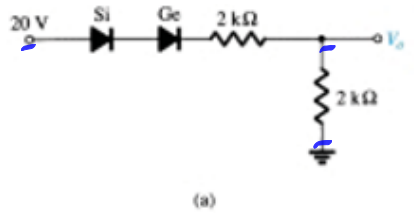
5. Determine the current I for each of the configurations of Fig. 2.134 using the approximate equivalent model for the diode.

	❖ Diode Reverse $I_D = 0$ mA
	❖ Diode Forward $I = \frac{19.3}{20} = 0.965$ A $I = \frac{0 - 0.7 - (-20)}{20}$
	❖ Center branch open $I = \frac{10\ V}{10\ \Omega} = 1$ A

6. Determine Vo and ID for the networks of Fig. 2.135.

	❖ Diode Forward Apply KVL $= -5\ V + 0.7\ V - V_0 = 0$ $V_0 = -4.3\ V$ $I_R = I_D = \frac{\lvert -4.3 \rvert}{2.2k} = 1.955$ mA
	❖ Diode Forward $I_D = \frac{8-0.7}{1.2k+4.7k} = 1.24$ mA $V_O = 0.7 + (1.24\ \text{mA} \times 4.7\ \text{k}\Omega) = 6.53$ V

7. Determine the level of Vo for each network of Fig. 2.136.

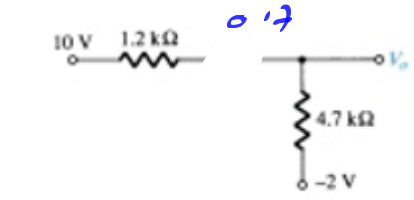


(a)

$$-20 + 0.7 + 0.3 + I_D R_1 + I_D R_2 = 0$$

$$I_D = \frac{20-0.7-0.3}{2k+2k} = 4.75 \text{ mA}$$

$$V_O = I_D R_2 = 4.75 \text{ mA} \times 2 \text{ k}\Omega = 9.5 \text{ V}$$



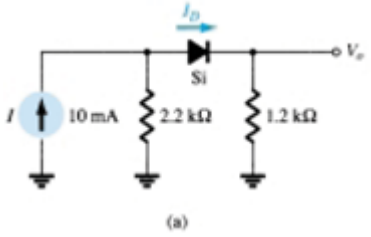
(b)

$$-10 + IR_1 + 0.7 + IR_2 - 2 = 0$$

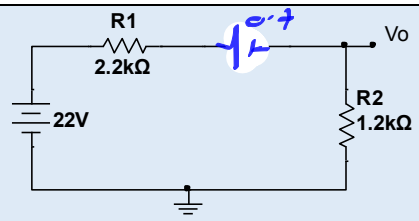
$$I_D = \frac{10+2-0.7}{1.2k+4.7k} = 1.915 \text{ mA}$$

$$V_O = (1.915 \text{ mA} \times 4.7 \text{ k}\Omega) - 2 = 9 - 2 = 7 \text{ V}$$

8. Determine Vo and ID for the networks of Fig. 2.137.



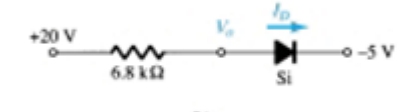
(a)



$$E = IR_1 = (10 \text{ mA})(2.2 \text{ k}\Omega) = 22 \text{ V}$$

$$\text{Apply KVL} = I_D = \frac{22-0.7}{2.2k+1.2k} = 6.26 \text{ mA}$$

$$V_O = (6.26 \text{ mA})(1.2 \text{ k}\Omega) = 7.51 \text{ V}$$



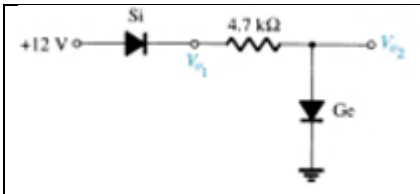
(b)

$$\text{Apply KVL} = -20 + I_D R + 0.7 - 5 = 0$$

$$I_D = \frac{20+5-0.7}{6.8k} = 3.6 \text{ mA}$$

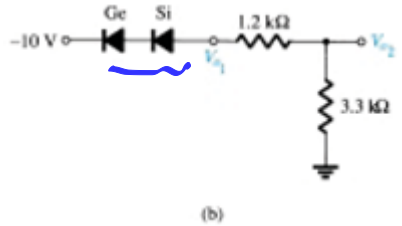
$$V_O = 20 - V_R = 20 - (3.6 \text{ mA} \times 6.8 \text{ k}\Omega) = 20 - 24.48 = -4.48 \text{ V}$$

9. Determine Vo1 and Vo2 for the networks of Fig. 2.138.



$$V_{O1} = E - V_{D1} = 12 - 0.7 = 11.3 \text{ V}$$

$$V_{O2} = V_{D2} = 0.3 \text{ V}$$



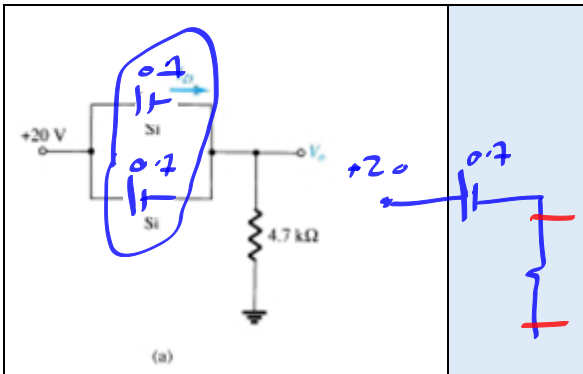
(b)

$$V_{O1} = -10 + 0.3 + 0.7 = -9 \text{ V}$$

$$\text{Apply KVL} = I_D = \frac{-10+0.3+0.7}{1.2k+3.3k} = -2 \text{ mA}$$

$$V_{O2} = (-2 \text{ mA} \times 3.3 \text{ k}\Omega) = -6.6 \text{ V}$$

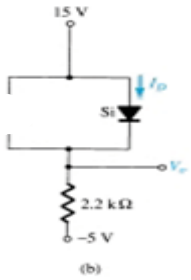
10. Determine Vo and ID for the networks of Fig. 2.139.

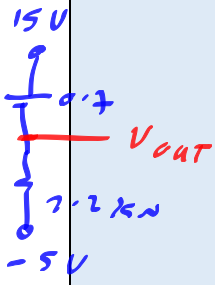


Apply KVL = $I = \frac{20-0.7}{4.7k} = 4.106$ mA

$I_D = \frac{I}{2} = 2.05$ mA

$V_O = IR = 4.106\text{ mA} \times 4.7\text{ k}\Omega = 19.3$ V

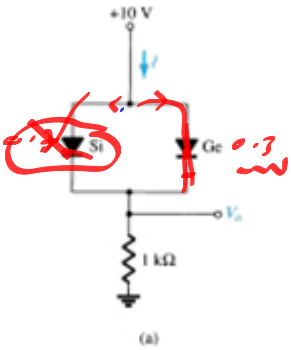


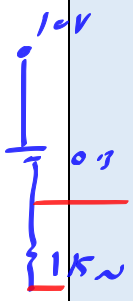


Apply KVL = $I_D = \frac{15+5-0.7}{2.2k} = 8.8$ mA

$V_O = 15 - 0.7 = 14.3$ V

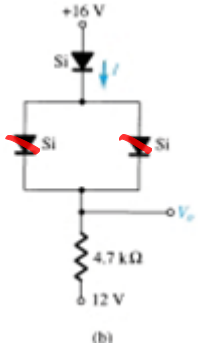
11. Determine Vo and I for the networks of Fig. 2.140.

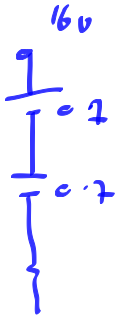




Ge diode FW and Si diode RW

$I_D = \frac{10 - 0.3}{1\ k\Omega} = 9.7$ mA





Apply KVL = $I = \frac{16-0.7-0.7-12}{4.7k} = 0.553$ mA

$V_O = 12\text{ V} + (0.553\text{ mA})(4.7\text{ k}\Omega) = 14.6$ V

12. Determine Vo1, Vo2, and I for the network of Fig. 2.141

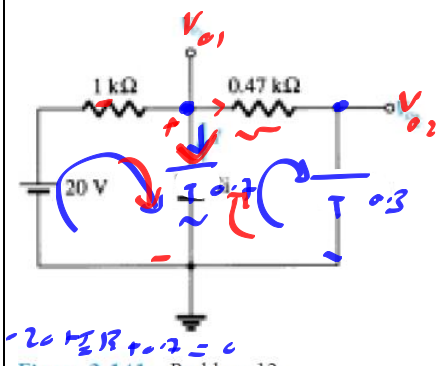


Figure 2.141 Problem 12

Both diodes FW

$V_{o1} = 0.7\ V\ \&\ V_{o2} = 0.3\ V$

$$I_{1k} = \frac{20-0.7}{1k} = 19.3\ mA$$

$$I_{0.47K} = \frac{0.7-0.3}{0.47k} = 0.851\ mA$$

$$I_{Si} = I_{1k} - I_{0.47k} = 19.3 - 0.851$$
$$= 18.45\ mA$$

13. Determine Vo and ID for the network of Fig. 2.142.

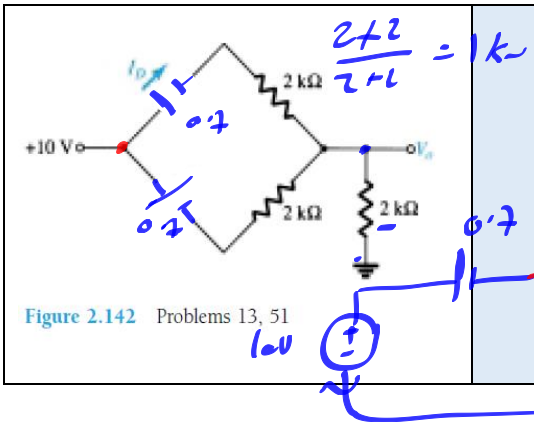


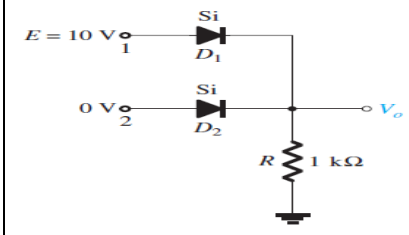
Figure 2.142 Problems 13, 51

$$\text{Apply KVL} = I = \frac{10-0.7}{1k+2k} = 3.1\ mA$$

$$V_O = (3.1\ mA)(2\ k\Omega) = 6.2\ V$$

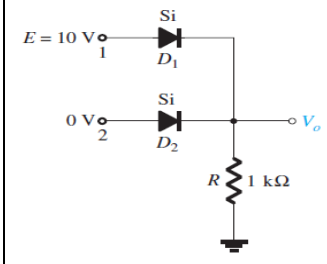
$$I_D = \frac{3.1}{2} = 1.55mA$$

14. Determine Vo for the network of Fig. 2.38 with 0 V on both inputs.



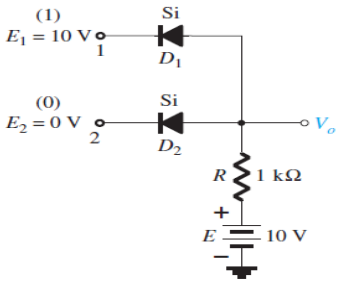
- ❖ both diodes RW
- ❖ $V_O = 0\ V = 0$ logic

15. Determine Vo for the network of Fig. 2.38 with 10 V on both inputs.



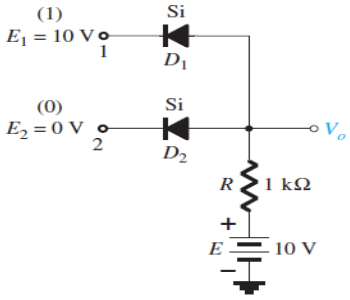
- ❖ both diodes FW
- ❖ $V_O = 10 - 0.7 = 9.3\ V = 1$ logic

16. Determine Vo for the network of Fig. 2.41 with 0 V on both inputs.



❖ both diodes FW
❖ $V_O = 0.7$ V = 0 logic

17. Determine Vo for the network of Fig. 2.41 with 10 V on both inputs.



❖ both diodes RW
❖ $V_O = 10$ V = 1 logic

18. Determine Vo for the negative logic OR gate of Fig. 2.143.

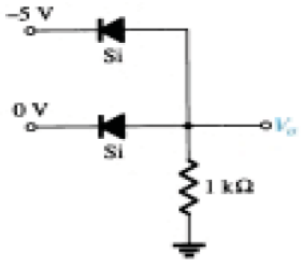


Figure 2.143 Problem 18

❖ first diode FW and second diode RW
❖ $V_O = -5 + 0.7 = -4.3$ V

19. Determine Vo for the negative logic AND gate of Fig. 2.144.

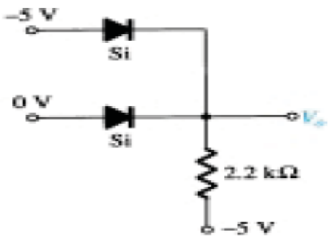


Figure 2.144 Problem 19

❖ first diode RW and second diode FW
❖ $V_O = 0 - 0.7 = -0.7$ V

20. Determine the level of Vo for the gate of Fig. 2.145.

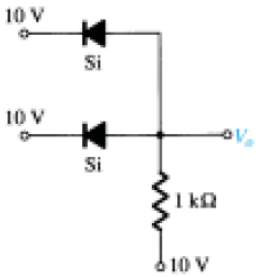


Figure 2.145 Problem 20

- both diodes RW
  - $V_O = 10$ V

21. Determine Vo for the configuration of Fig. 2.146.

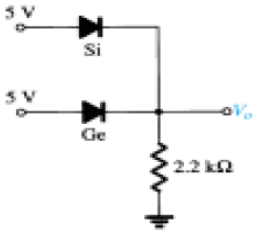
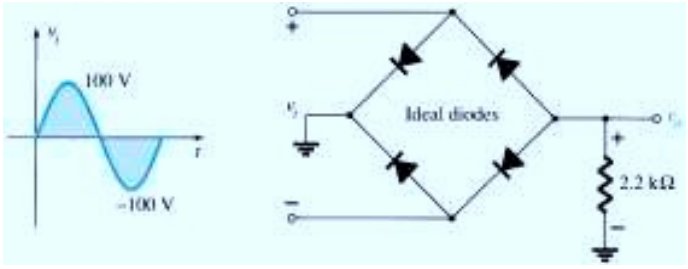


Figure 2.146 Problem 21

- Si diode RW and Ge diode FW
  - $V_O = 5 - 0.3 = 4.7$ V

Assigment-1 (CLO-1)

29. Determine v_o and the required PIV rating of each diode for the configuration of Fig. 2.152.



For the positive half-cycle of the input, diodes D_1 and D_3 are forward biased and diodes D_2 and D_4 are reverse biased as shown in Figure.

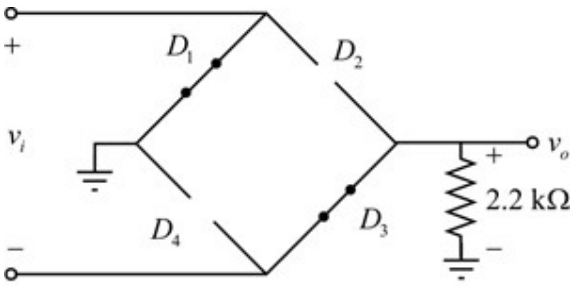


Figure 1

the output voltage is,

$$v_o = -v_i$$

For the negative half-cycle of the input, diodes D_2 and D_4 are forward biased and diodes D_1 and D_3 are reverse biased as shown in Figure .

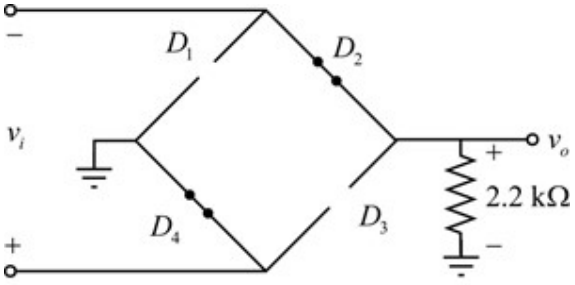


Figure 2

Hence for the negative half-cycle, the output voltage is,

$v_o = v_i$

The output voltage v_o is shown in Figure 3.

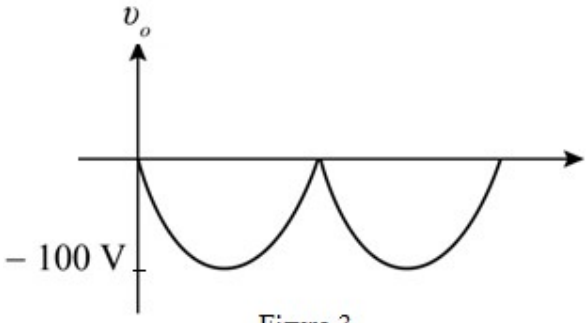


Figure 3

The PIV is defined as the maximum voltage across the diodes in the reverse bias.

Therefore, the required PIV rating for each of the Ideal diodes is $\boxed{100\text{ V}}$.

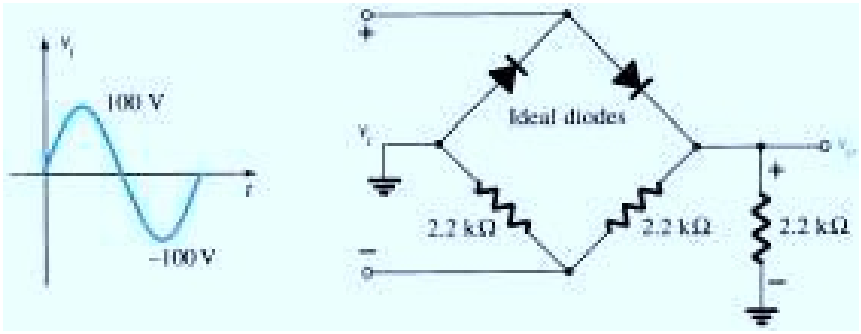
Calculate the maximum current I_{max} through each diode.

$$I_{max} = \frac{-v_o(\text{peak})}{R} \quad \ldots\ldots (1)$$

Substitute $2.2\text{ k}\Omega$ for R and -100 V for $v_o(\text{peak})$.

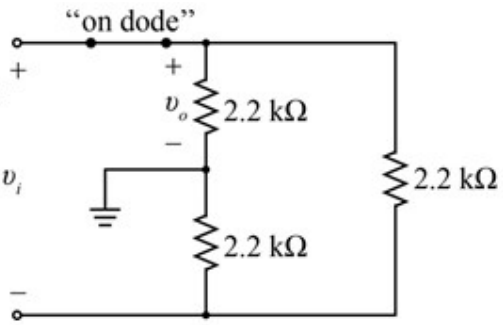
$$I_{max} = \frac{-(-100)}{2.2\text{ k}\Omega}$$
$$= \frac{100\text{ V}}{2.2\text{ k}\Omega}$$
$$= 45.45\text{ mA}$$

* **30.** Sketch v_o for the network of Fig. 2.153 and determine the dc voltage available.



draw circuit for the Positive half cycle.

Network redrawn:



The maximum voltage $V_{i_{max}}$ 100 V .

Apply voltage divider rule to the circuit shown in Figure 1.

$$V_{o_{max}} = \frac{2.2\ \text{k}\Omega\left(V_{i_{max}}\right)}{2.2\ \text{k}\Omega + 2.2\ \text{k}\Omega}$$

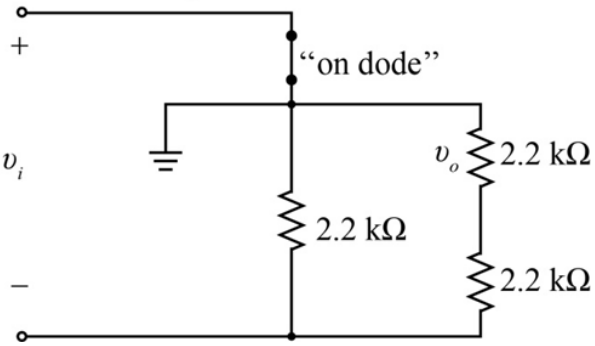
$$= \frac{1}{2}V_{i_{max}}$$

$$= \frac{1}{2}(100\ \text{V})$$

$$= 50\ \text{V}$$

Draw the circuit diagram for the Negative half cycle.

Network half-cycle of v_i:



The polarity of output voltage v_o across the $2.2\ \text{k}\Omega$ resistor is the same.

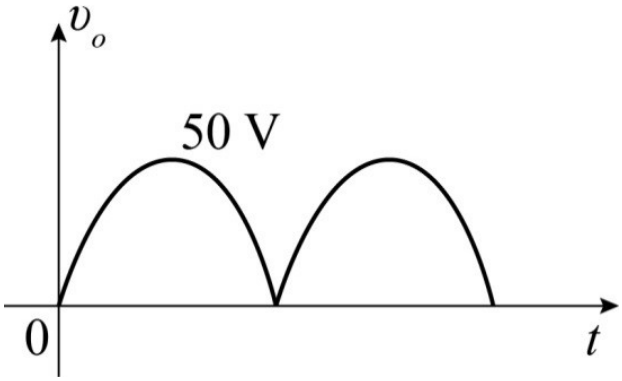
Apply voltage divider rule to the circuit shown in Figure 2.

$$\begin{aligned} V_{o_{\max}} &= \frac{2.2\ \text{k}\Omega\left(V_{i_{\max}}\right)}{2.2\ \text{k}\Omega + 2.2\ \text{k}\Omega} \\ &= \frac{1}{2}V_{i_{\max}} \\ &= \frac{1}{2}(100\ \text{V}) \\ &= 50\ \text{V} \end{aligned}$$

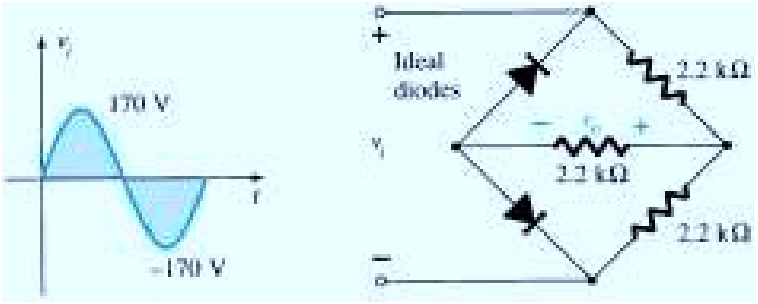
The direct current voltage V_{dc} is given as follows:

$$\begin{aligned} V_{dc} &= 0.636V_m \\ &= 0.636(50\ \text{V}) \\ &= 31.8\ \text{V} \end{aligned}$$

Draw the output waveform.



* **31.** Sketch v_o for the network of Fig. 2.154 and determine the dc voltage available.



for the Positive Pulse for the input voltage v_i the top left diode is forward biase and the bottom left is reverse biase.

$$V_{o_{peak}} = \frac{R_{net}(V)}{R_{net} + R}$$

$$\begin{aligned} R_{net} &= R \,\|\, R \\ &= 2.2\ \text{k}\Omega \,\|\, 2.2\ \text{k}\Omega \quad [R = 2.2\ \text{k}\Omega] \\ &= 1.1\ \text{k}\Omega \end{aligned}$$

$$\begin{aligned} V_{o_{peak}} &= \frac{R_{net}(V)}{R_{net} + R} \\ &= \frac{1.1\ \text{k}\Omega(170\ \text{V})}{1.1\ \text{k}\Omega + 2.2\ \text{k}\Omega} \\ &= 56.67\ \text{V} \end{aligned}$$

for the Negative Pulse for the input voltage v_i the top left diode is forward biase state and the bottom left is reverse biase.

$$\begin{aligned} R_{net} &= R \,\|\, R \\ &= 2.2\ \text{k}\Omega \,\|\, 2.2\ \text{k}\Omega \quad [R = 2.2\ \text{k}\Omega] \\ &= 1.1\ \text{k}\Omega \end{aligned}$$

$$\begin{aligned} V_{o_{peak}} &= \frac{R_{net}(V)}{R_{net} + R} \\ &= \frac{1.1\ \text{k}\Omega(170\ \text{V})}{1.1\ \text{k}\Omega + 2.2\ \text{k}\Omega} \\ &= 56.67\ \text{V} \end{aligned}$$

Sketch the output voltage v_o as shown in Figure .

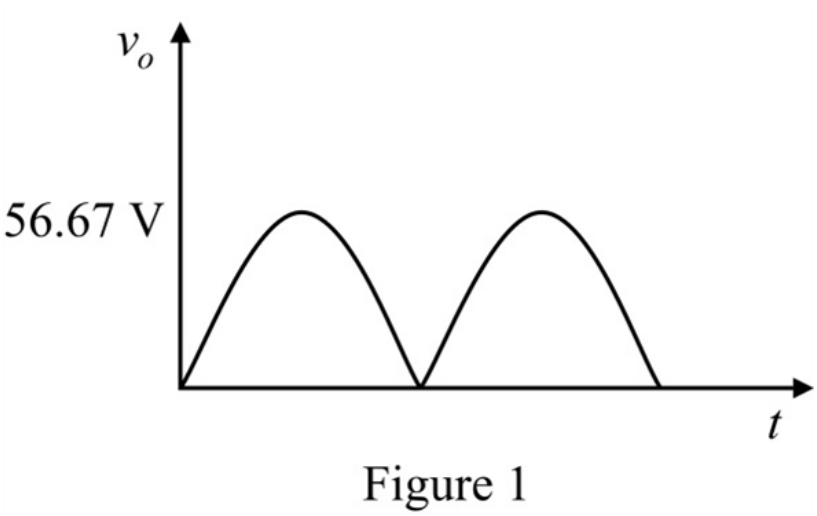


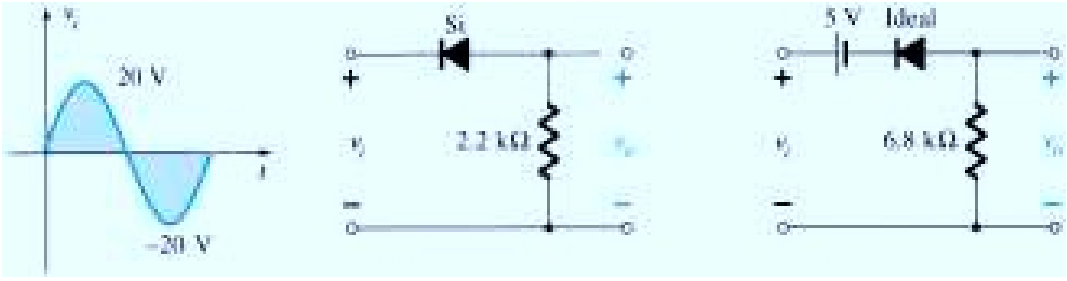
Figure 1

Determine the dc-voltage V_{dc}.

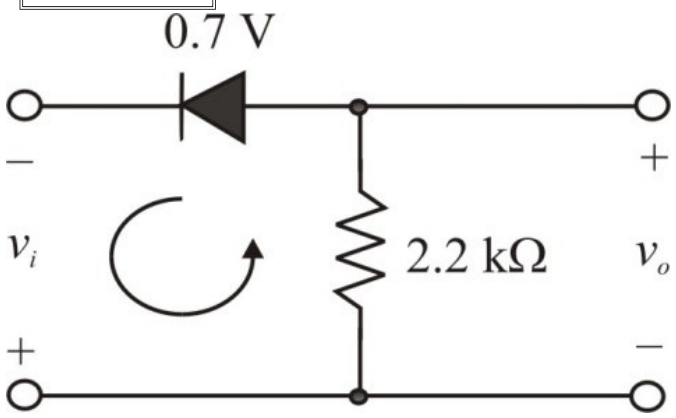
For a full-wave rectifier the dc-voltage is,

$$V_{dc} = 0.636\left(V_{o_{peak}}\right)$$
$$= 0.636(56.67\ \text{V})$$
$$= 36.04\ \text{V}$$

32. Determine v_o for each network of Fig. 2.155 for the input shown.



the diode will conduct during the negative part of the input signal. The circuit is redrawn as shown in Figure.



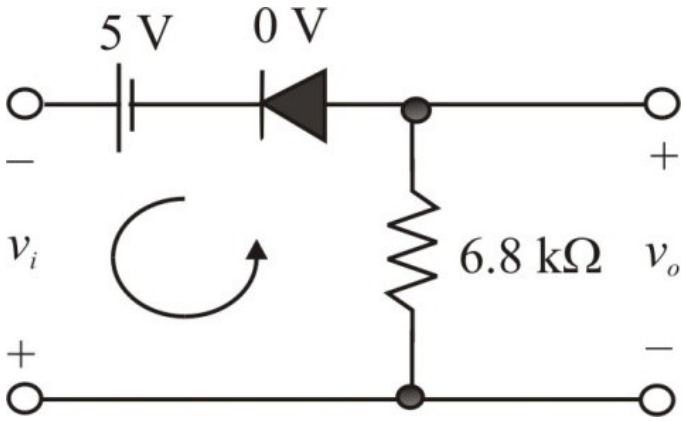
For the Silicon diode, the threshold voltage is 0.7 V. The voltage across the resistor is v_o. Apply the Kirchhoff's voltage law (KVL) around the input loop.

$$-v_i - v_o + 0.7\,\text{V} = 0$$

Calculate the output voltage by substituting $20\,\text{V}$ for v_i.

$$\begin{aligned} -v_i - v_o + 0.7\,\text{V} &= 0 \\ v_o &= -v_i + 0.7\,\text{V} \\ &= -20\,\text{V} + 0.7\,\text{V} \\ &= -19.3\,\text{V} \end{aligned}$$

, the diode will conduct during the negative part of the input signal. The circuit is redrawn as shown in Figure .



For the ideal diode, the threshold voltage is 0 V. The voltage across the resistor is v_o. Apply the Kirchhoff's voltage law (KVL) around the input loop.

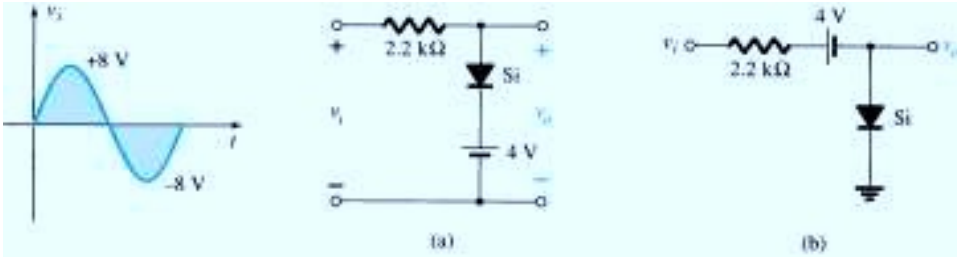
$$-v_i - v_o + +0 - 5\,\text{V} = 0$$

Calculate the output voltage by substituting $20\,\text{V}$ for v_i.

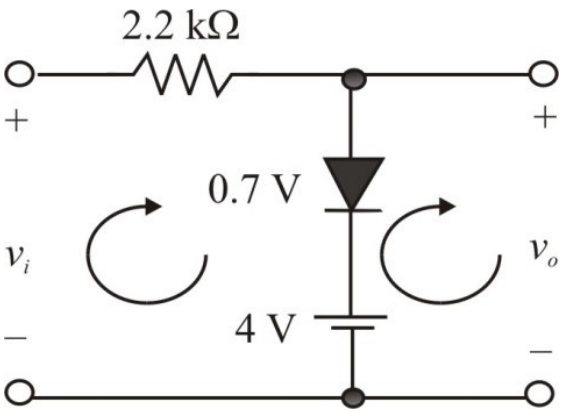
$$-v_i - v_o + 0 - 5\,\text{V} = 0$$

$$v_o = -v_i - 5\,\text{V}$$
$$= -20\,\text{V} - 5\,\text{V}$$
$$= -25\,\text{V}$$

* **35.** Determine v_o for each network of Fig. 2.158 for the input shown.



(a) the diode will conduct during the positive part of the input signal. The threshold voltage of the Silicon diode is 0.7 V. The circuit is redrawn as shown in Figure.



Apply the Kirchhoff's voltage law (KVL) around the outer loop.

$$-4\,\text{V} - 0.7\,\text{V} + v_o = 0$$

$$-4\,\text{V} - 0.7\,\text{V} + v_o = 0$$
$$v_o = 4\,\text{V} + 0.7\,\text{V}$$
$$= 4.7\,\text{V}$$

(b)

The output voltage is taking across diode during the positive part of the input signal. Hence the output voltage is equal to the threshold voltage of the diode, which is 0.7 V.

The output voltage during the negative part of the input signal is the sum of the input voltage and the battery voltage.

Hence the output voltage is equals as follows.

$$v_o = -8\,\text{V} - 4\,\text{V}$$
$$= -12\,\text{V}$$

36. Sketch IR and Vo for the network of Fig. 2.159 for the input shown.

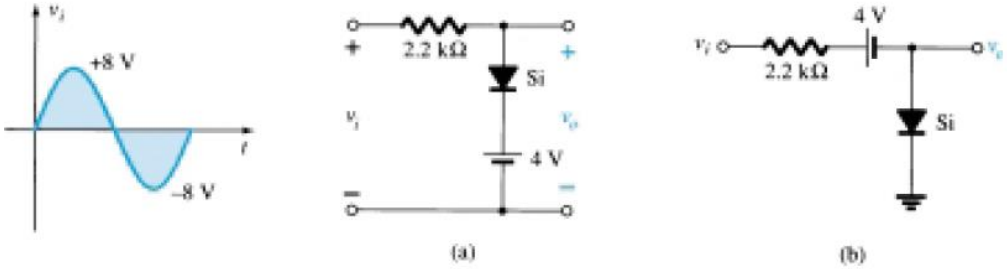


Figure 2.158 Problem 35

V_0

- at the positive of Vin :

D1 is FW at Vin > (5.3 + 0.7)

D2 is RW

- at the negative of Vin :

D1 is RW

D2 is FW at Vin < (–7.3 – 0.7)

I_R

- Vi ≥ 6 , (D1 is FW)

VR = Vi – Vo = Vi – 6

Vi = 10 V , VR = 4 V

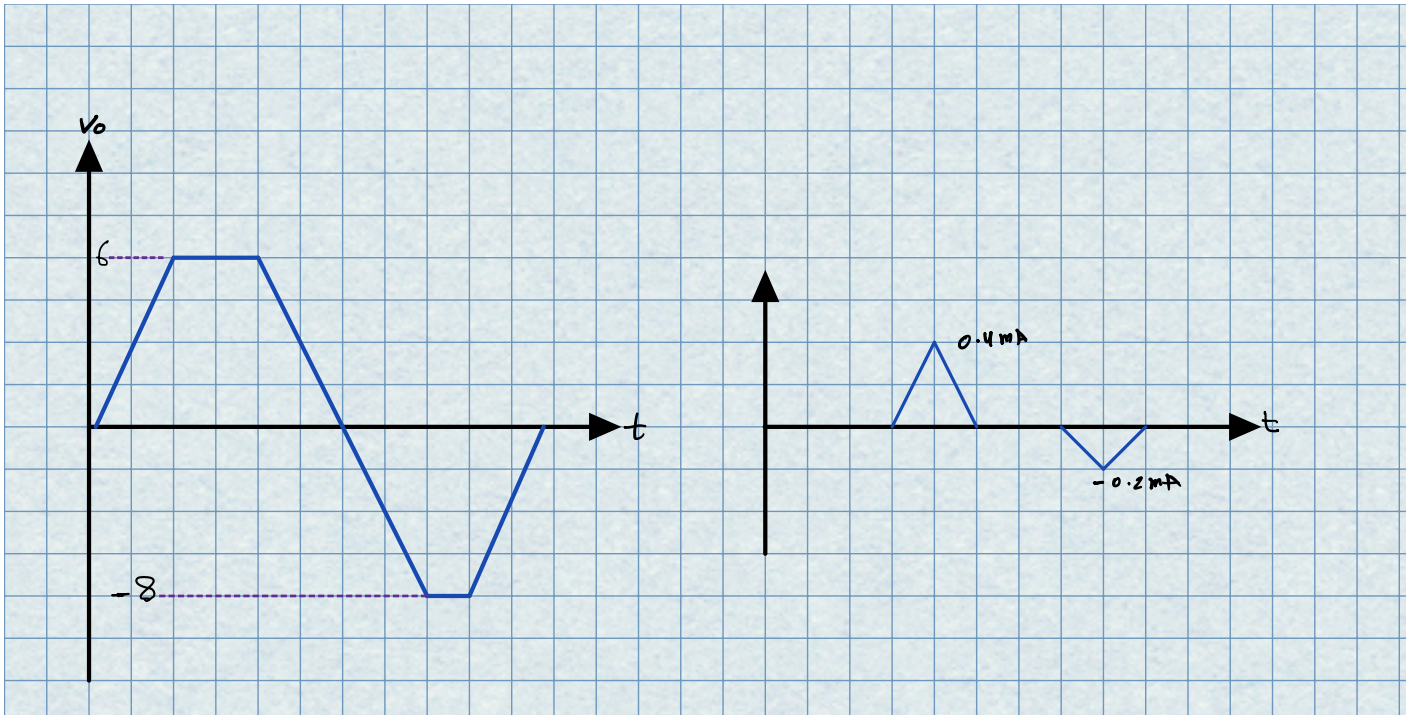
$$I_R = \frac{4}{10} = 0.4mA$$

- Vi ≥ – 8 , (D2 is FW)

VR = Vi – Vo = Vi + 8

Vi = -10 V , VR = -2V

$$I_R = \frac{-2}{10} = -0.2mA$$



37. Sketch Vo for each network of Fig. 2.160 for the input shown.

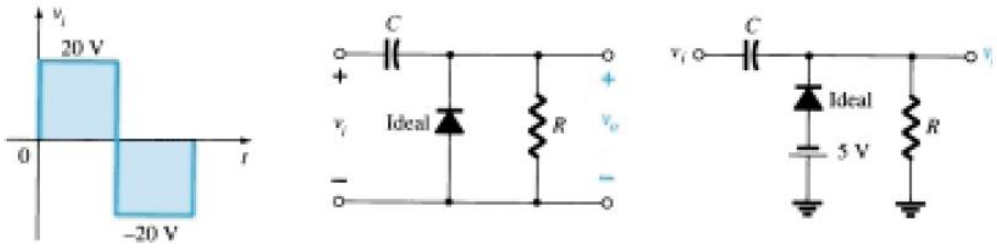
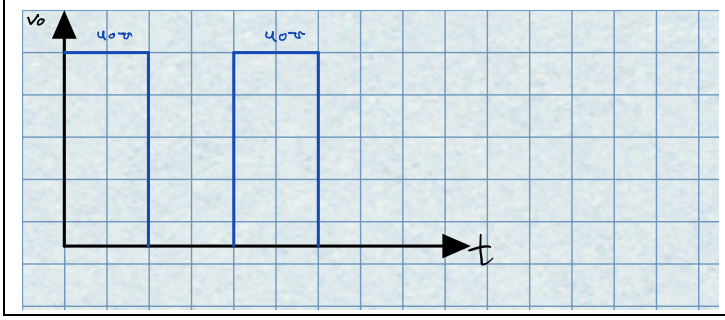
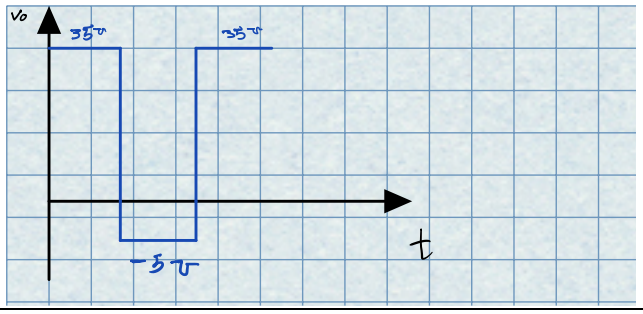


Figure 2.160 Problem 37

The negative of Vin , diode is FW and capacitor charges VC = 20 V and Vo = 0 V The positive of Vin , diode is RW and capacitor discharges Vo = Vin + VC = 20 + 20 = 40 V	The negative of Vin , diode is FW and capacitor charges VC = 15 V and Vo = – 5 V The positive of Vin , diode is RW and capacitor discharges Vo = Vin + VC = 20 + 15 = 35 V
	

38. Sketch Vo for each network of Fig. 2.161 for the input shown. Would it be a good approximation to consider the diode to be ideal for both configurations? Why?

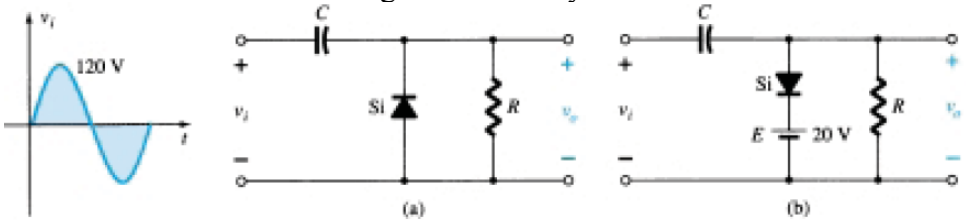
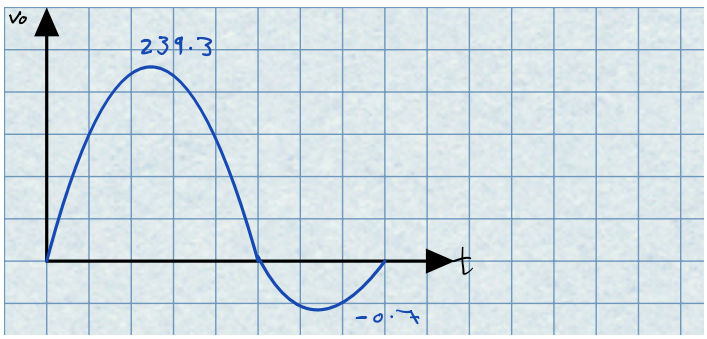
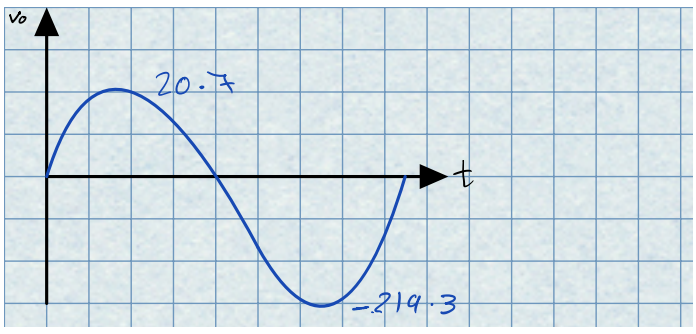


Figure 2.161 Problem 38

The negative of Vin , diode is FW and capacitor charges VC = 119.3 V and Vo = 0.7 V The positive of Vin , diode is RW and capacitor discharges Vo = Vin + VC = 120 + 119.3 = 239.3 V	The positive of Vin , diode is FW and capacitor charges VC = 99.3 V and Vo = 20.7 V The negative of Vin , diode is RW and capacitor discharges Vo = -120 – 99.3 = -219.3 V
	

39. For the network of Fig. 2.162:

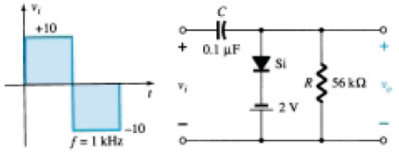
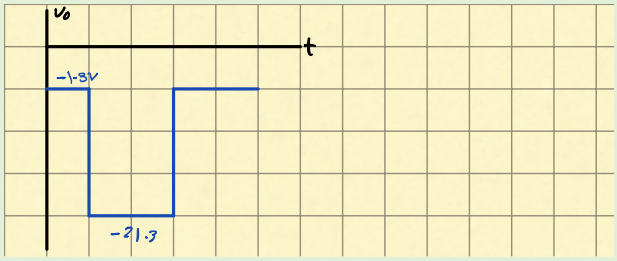


Figure 2.162 Problem 39

(a) Calculate 5τ.
5τ = 5 × RC = 5 × (56 kΩ)(0.1 μF) = 28 ms
(b) Compare 5τ to half the period of the applied signal.
Half the period = 0.5 ms and 5τ = 28 ms = 56:1
(c) Sketch Vo.

❖ The positive of Vin , diode is FW and capacitor charges.
VC = 11.3 V and Vo = – 1.3 V

❖ The negative of Vin , diode is RW and capacitor discharges.
Vo = – 10 – 11.3 = – 21.3 V



42.

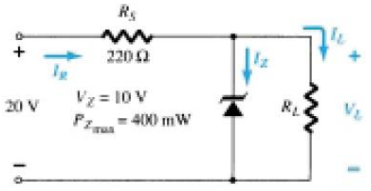
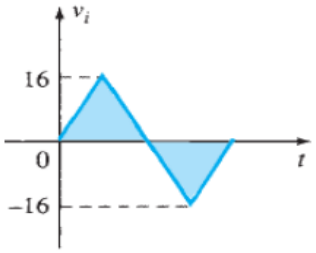


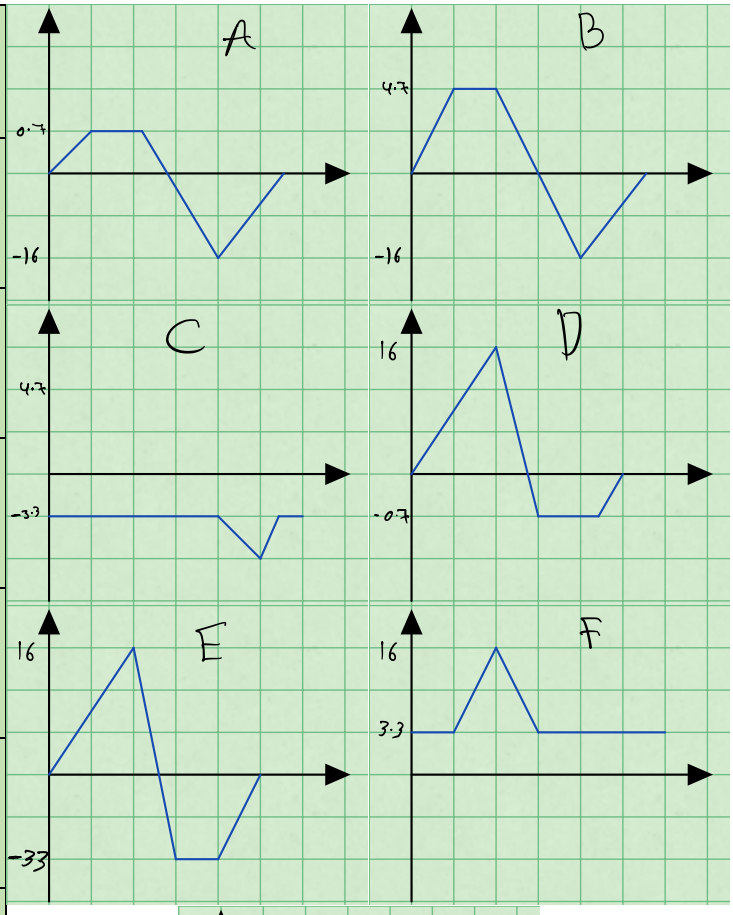
Figure 2.165 Problem 42

(a) Determine VL, IL, IZ, and IR for the network Fig. 2.165 if RL = 180 Ω
$V_L = V_{in}\frac{R_L}{R_L + R_s} = 20\frac{180}{180 + 220} = 9\ V\ and\ diode\ is\ RW$ $I_R = \frac{20}{220 + 180} = 50\ mA$
(b) Repeat part (a) if RL = 470 Ω.
$V_L = 20\frac{470}{470 + 220} = 13.62\ V\ and\ diode\ is\ FW$ $I_L = \frac{10}{470} = 21.28\ mA\ \ and\ I_R = \frac{10}{220} = 45.45\ mA$ $I_Z = 45.45 - 21.28 = 24.17\ mA$
(c) Determine the value of RL that will establish maximum power conditions for the Zener diode.
$P_{Zmax} = \frac{400\ mW}{10\ V} = 40\ mA \qquad I_{Lmin} = 45.45 - 40 = 5.45\ mA$ $RL = \frac{10\ V}{5.45\ mA} = 1834.86\Omega$
(d) Determine the minimum value of RL to ensure that the Zener diode is in the "on" state.
$V_L = V_{in}\frac{R_L}{R_L + R_s}\ so\ 10 = 20\frac{R_L}{R_L + 220} = R_L = 220\Omega$

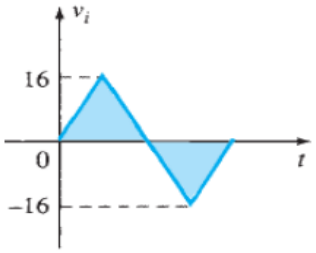
Use the 7 cases of parallel clippers that we cover in lecture to sketch VO for the following input signal and use a 4 V battery.



A	$Diode\ FW\ at\ V_{in} > 0.7$ $Diode\ RW\ at\ V_{in} < 0.7$
B	$Diode\ FW\ at\ V_{in} > (4 + 0.7)$ $Diode\ RW\ at\ V_{in} < (4 + 0.7)$
C	$Diode\ FW\ at\ V_{in} > (0.7 - 4)$ $Diode\ RW\ at\ V_{in} < (0.7 - 4)$
D	$Diode\ FW\ at\ V_{in} > -0.7$ $Diode\ RW\ at\ V_{in} < -0.7$
E	$Diode\ FW\ at\ V_{in} < (0.7 - 4)$ $Diode\ RW\ at\ V_{in} > (0.7 - 4)$
F	$Diode\ FW\ at\ V_{in} < (4 - 0.7)$ $Diode\ RW\ at\ V_{in} > (4 - 0.7)$
G	$D_1 FW\ at\ V_{in} > (4 + 0.7)$ $D_2\ FW\ at\ V_{in} < (-4 - 0.7)$



Use the 6 cases of clampers that we cover in lecture to sketch VO for the following input signal and use a 4 V battery.



A	$Diode\ FW\ at + V_{in}$ $V_C = 16\ V\ \&\ V_O = 0\ V$ $Diode\ RW\ at - V_{in}$ $V_O = -32\ V$
B	$Diode\ FW\ at - V_{in}$ $V_C = 16\ V\ \&\ V_O = 0\ V$ $Diode\ RW\ at + V_{in}$ $V_O = 32\ V$
C	$Diode\ FW\ at + V_{in}$ $V_C = 12\ V\ \&\ V_O = 4\ V$ $Diode\ RW\ at - V_{in}$ $V_O = -28\ V$
D	$Diode\ FW\ at - V_{in}$ $V_C = 20\ V\ \&\ V_O = 4\ V$ $Diode\ RW\ at + V_{in}$ $V_O = 36\ V$
E	$Diode\ FW\ at + V_{in}$ $V_C = 20\ V\ \&\ V_O = -4\ V$ $Diode\ RW\ at - V_{in}$ $V_O = -36\ V$
F	$Diode\ FW\ at - V_{in}$ $V_C = 12\ V\ \&\ V_O = -4\ V$ $Diode\ RW\ at + V_{in}$ $V_O = 28\ V$