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. مقاطع فيديوهات لشرح المقرر بشكل وافي
. ملخص للمادة Pdf للمذكرة والمراجعة
. محاضرات مباشرة علي برنامج زووم
لمناقشة الأجزاء الغير مفهومة
. تواصل مستمر مع معلم المادة
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ميكانيكا الانشائات
هيدروليكا

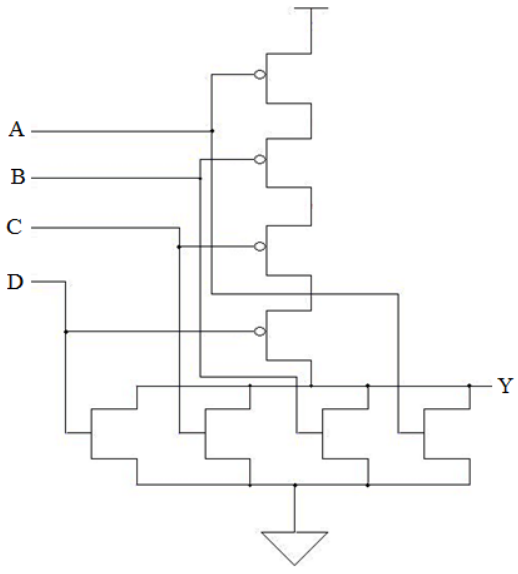
1.5 Sketch a transistor-level schematic for a CMOS 4-input NOR gate

the truth table for a 4-input NOR gate.

W	X	Y	Z	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Figure 1: Truth table for 4-input NOR gate.

Observe from the truth table that the output is high when all of the input are low and that the output is low when at least one of the inputs is high. This means that in the transistor schematic, the PMOS transistors must be in series and the NMOS transistors must be in



Observe from the schematic that when all of the inputs are low the 4 NMOS transistors are turned off so there is connection between the output and ground. The 4 PMOS transistors on the other hand will all be on so the output will get pulled up to V_{DD}. If one of the inputs is

high then the output cannot get pulled up to V_{DD}; instead one of the NMOS transistors will be turned on and the output will be pulled down to ground. Therefore this schematic acts exactly like a 4 input NOR gate.

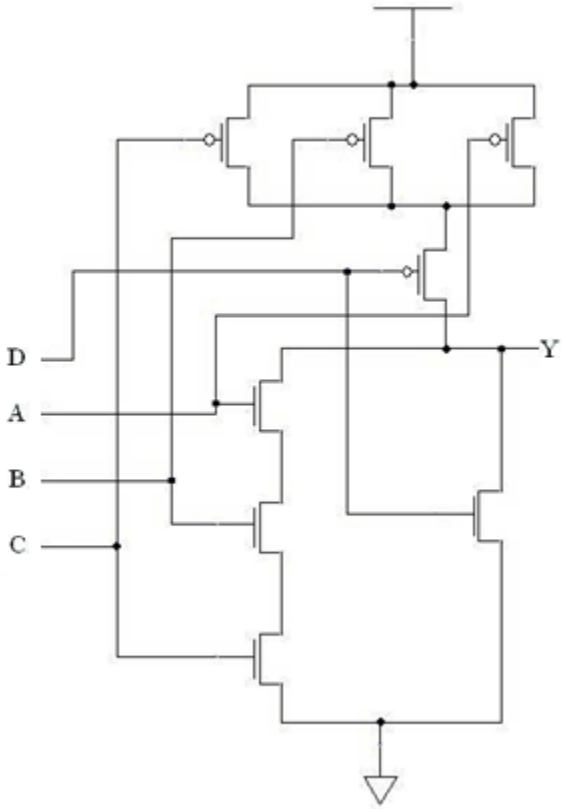
1.6 Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following functions:

a) $\boldsymbol{Y = \overline{ABC + D}}$

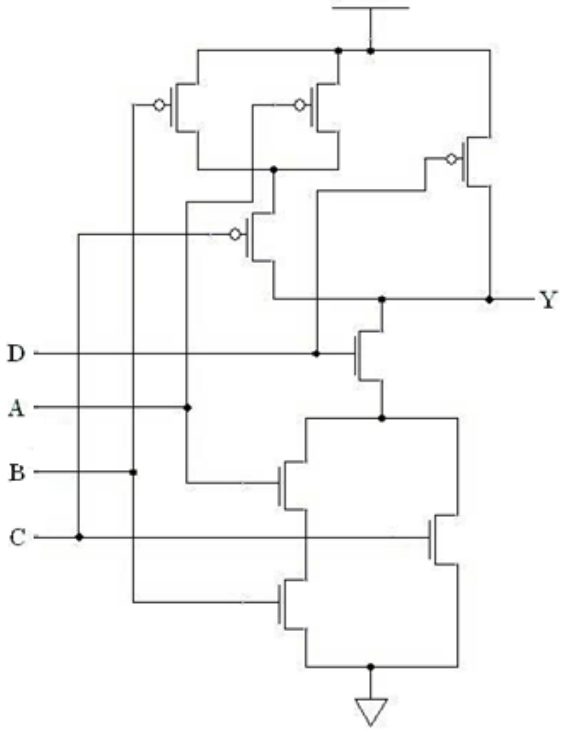
b) $\boldsymbol{Y = \overline{(AB + C) \cdot D}}$

c) $\boldsymbol{Y = \overline{AB + C \cdot (A + B)}}$

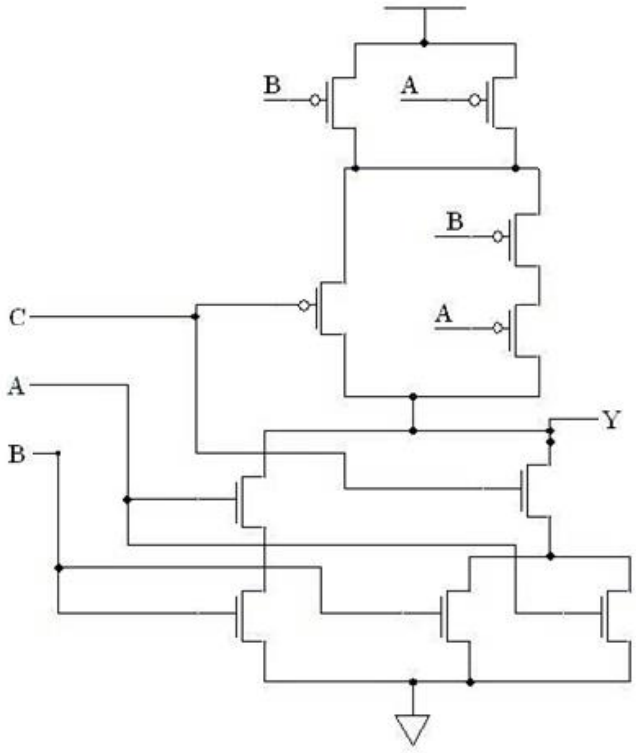
(a) $Y = \overline{ABC + D}$



(b) $Y = \overline{(AB + C) \cdot D}$



(c) $Y = \overline{AB + C \cdot (A + B)}$



1.7 Use a combination of CMOS gates (represented by their symbols) to generate the following functions from A, B, and C.

a) Y = A (buffer)

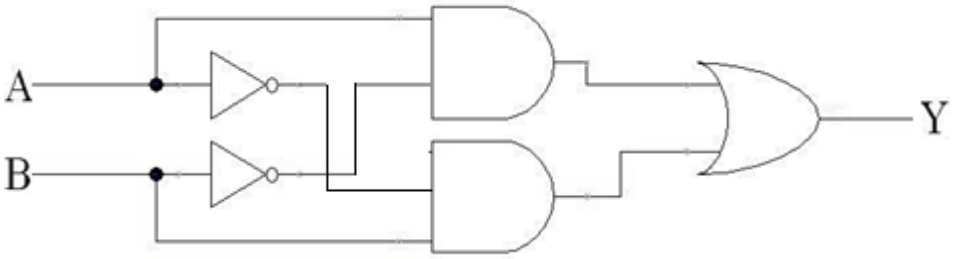
b) Y = $A\overline{B} + \overline{A}B$ (XOR)

c) Y = $\overline{A}\ \overline{B} + AB$ (XNOR)

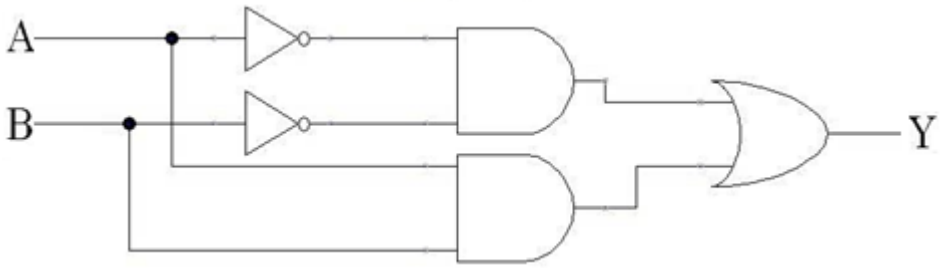
d) Y = AB + BC + AC (majority)

(a)

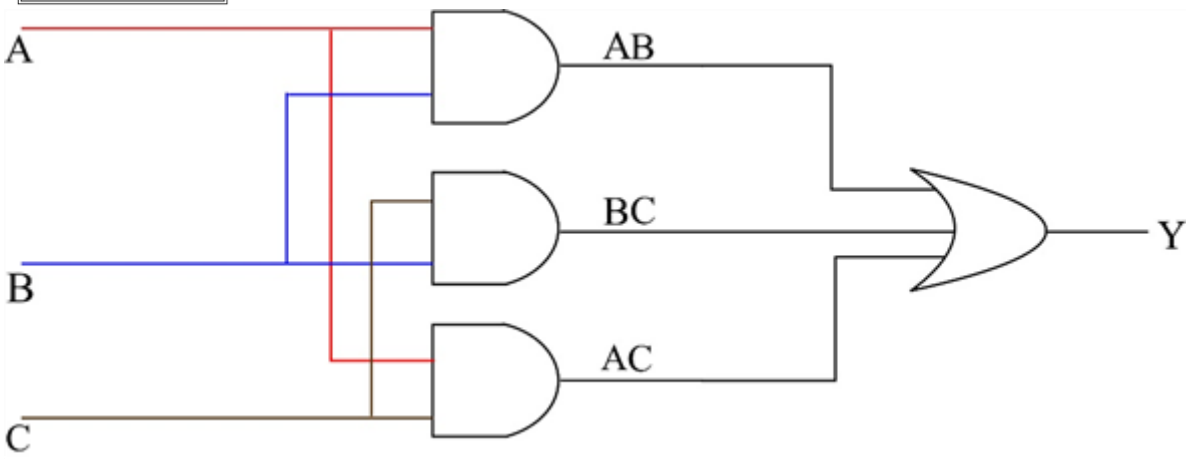
(b)



(c)



(d)



1.9 Sketch transistor-level schematics for the following logic functions. You may assume you have both true and complementary versions of the inputs available.

a) A 2:4 decoder defined by

$Y0 = \overline{A0} \cdot \overline{A1}$

$Y1 = A0 \cdot \overline{A1}$

$Y2 = \overline{A0} \cdot A1$

$Y3 = A0 \cdot A1$

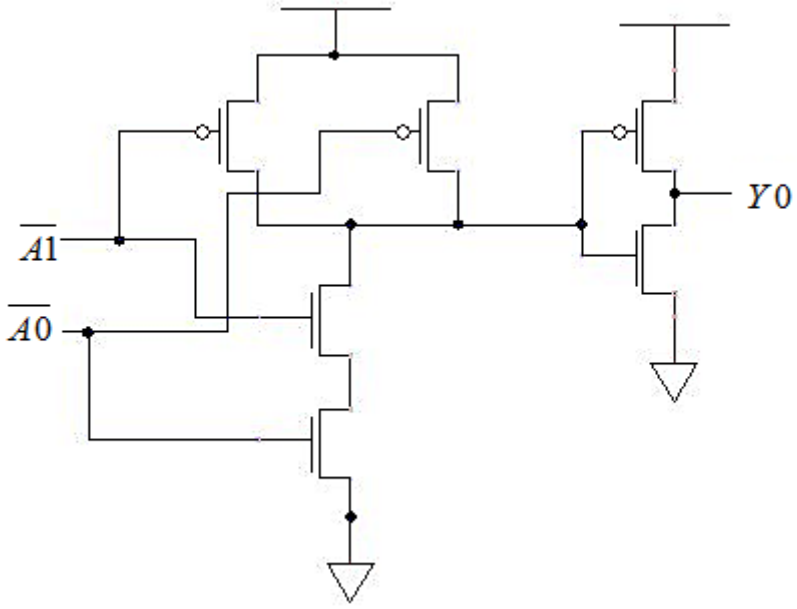
b) A 3:2 priority encoder defined by

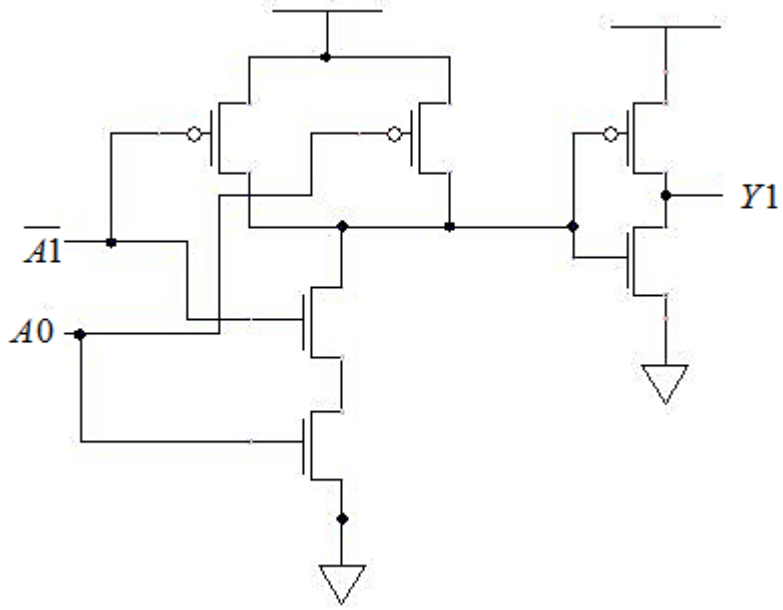
$Y0 = \overline{A0} \cdot (A1 + \overline{A2})$

$Y1 = \overline{A0} \cdot \overline{A1}$

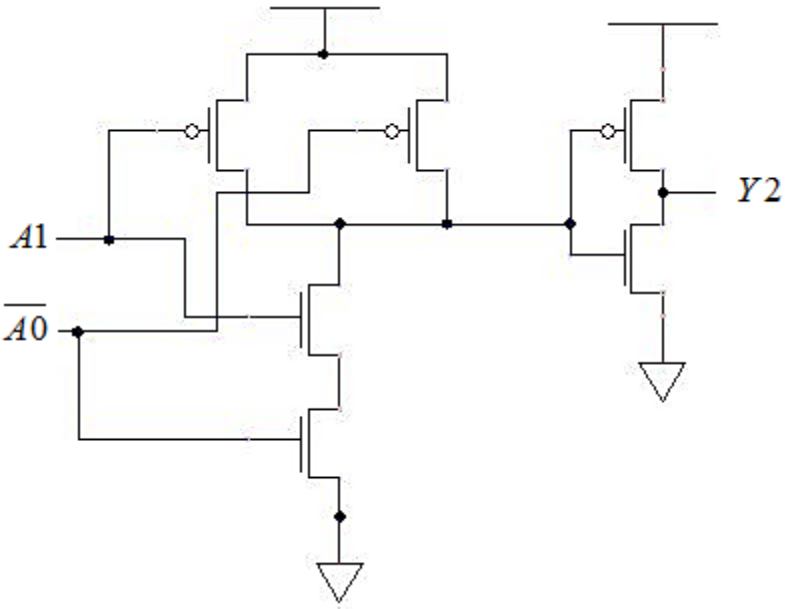
(a)

$Y0 = \overline{A0} \cdot \overline{A1}$

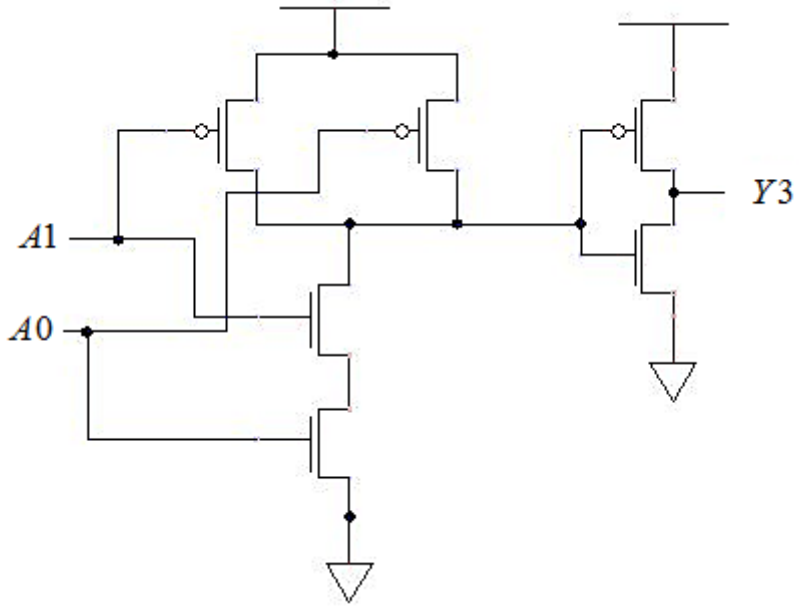




$$Y2 = \overline{A0} \cdot A1$$



$Y3 = A0 \cdot A1$



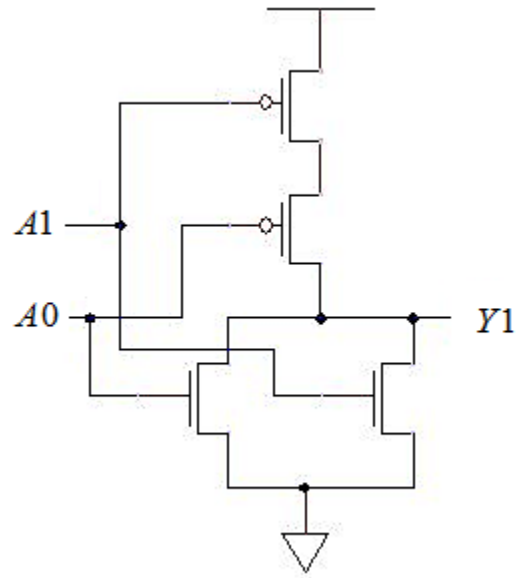
(b)

$Y0 = \overline{A0} \cdot \left(A1 + \overline{A2} \right)$

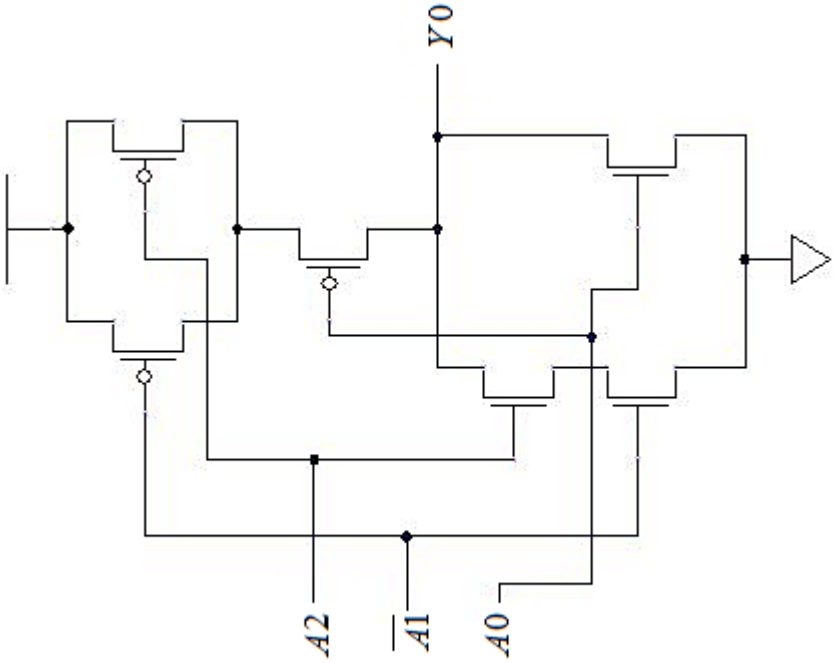
$Y1 = \overline{A0} \cdot \overline{A1}$

$Y1 = \overline{A0} \cdot \overline{A1}$

$= \overline{A0 + A1}$



$$Y0 = \overline{A0}\cdot\left(A1 + \overline{A2}\right)$$
$$= \overline{A0 + \left(\overline{A1} + \overline{\overline{A2}}\right)}$$
$$= \overline{A0 + \left(\overline{A1}\cdot A2\right)}$$



1.10 Sketch a stick diagram for a CMOS 4-input NOR gate from Exercise 1.5.

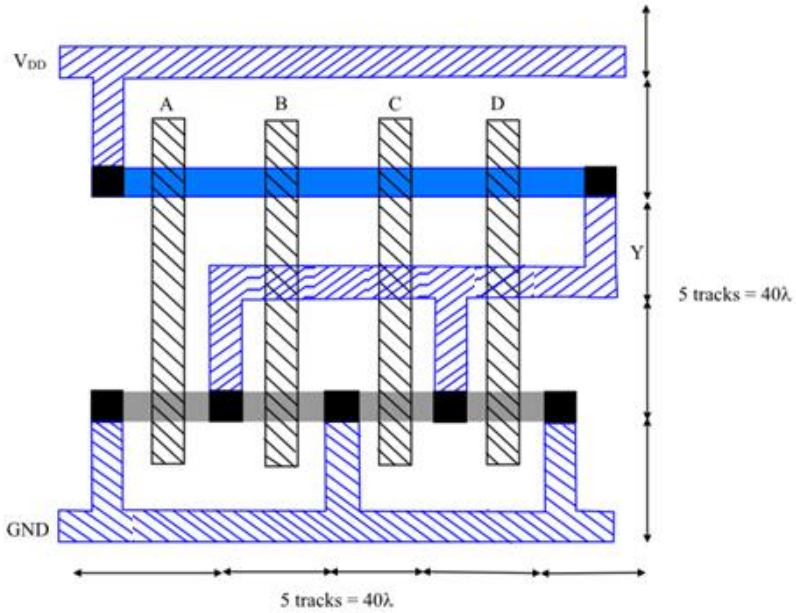


Figure 2

1.16 Consider the design of a CMOS compound OR-AND-INVERT (OAI21) gate computing $F = \overline{(A + B) \cdot C}$.

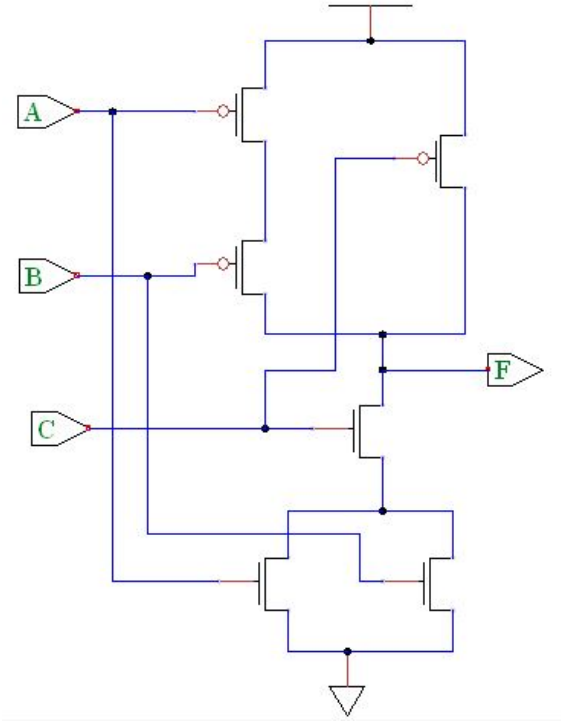
a) sketch a transistor-level schematic

b) sketch a stick diagram

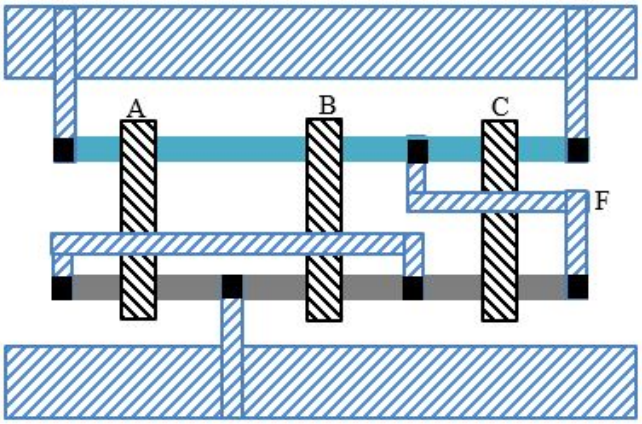
c) estimate the area from the stick diagram

d) layout your gate with a CAD tool using unit-sized transistors e) compare the layout size to the estimated area.

(a)



(b)



(c)

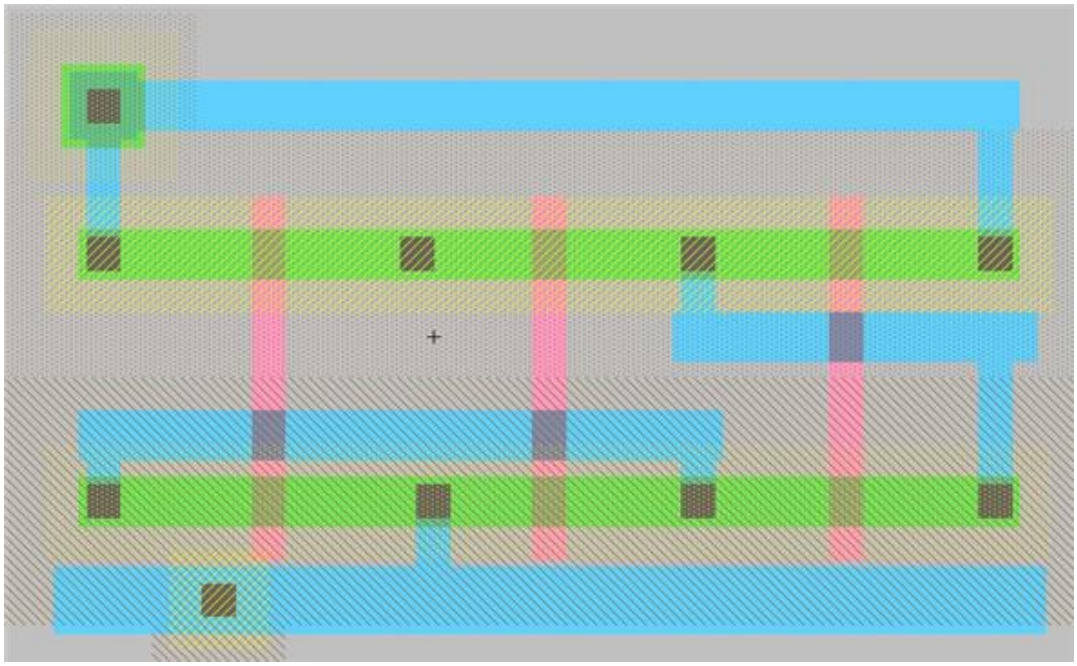
For the stick diagram in Figure 2 observe that horizontally it has 4 metal rectangles in a row. Now if each rectangle is 4λ wide and the spacing between them is 4λ then the minimum width is 32λ.

Vertically the diagram has 6 metal rectangles so if each rectangle is 4λ tall and the spacing between them is 4λ then the minimum height is 48λ. The width and height of the stick diagram get an estimate of the area of the layout.

$$\begin{aligned} A &= WH \\ &= (32\lambda)(48\lambda) \\ &= 1536\lambda^2 \end{aligned}$$

(d)

The layout diagram of the circuit in CAA tool is shown in Figure 3:



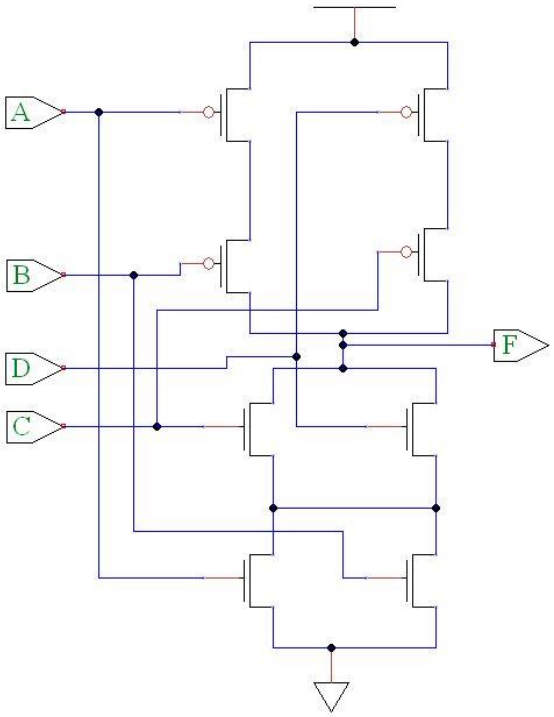
(e)

Now measure the area of layout and compare it to the area estimate from the stick diagram. Recall that λ is just half of the minimum width of a transistor in the process. The actual layout area and its estimate should match or at least be very close. The layout shown in Figure 3 has an area that matches the estimate.

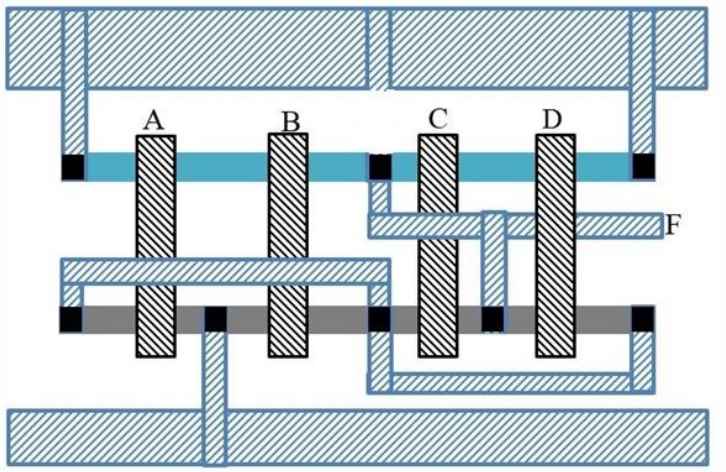
1.17 Consider the design of a CMOS compound OR-OR-AND-INVERT (OAI22) gate computing $F = \overline{(A + B) \cdot (C + D)}$.

a) sketch a transistor-level schematic
b) sketch a stick diagram
c) estimate the area from the stick diagram
d) layout your gate with a CAD tool using unit-sized transistors
e) compare the layout size to the estimated area

(a)



(b)



(c)

From Figure 2, observe that horizontally it has 5 metal rectangles in a row. Now if each rectangle is 4λ wide and the spacing between them is 4λ then the minimum width is 40λ.

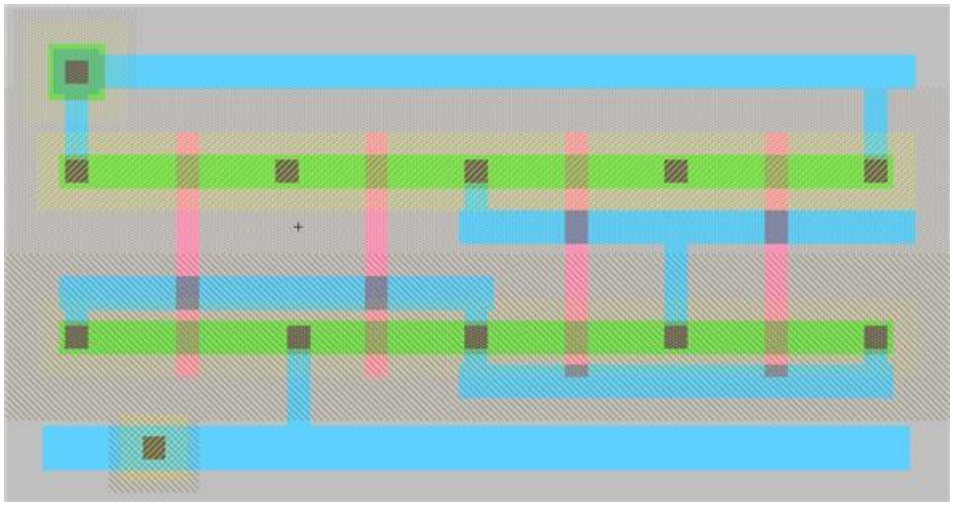
Vertically the diagram has 6 metal rectangles so if each rectangle is 4λ tall and the spacing between them is 4λ then the minimum height is 48λ.

Calculate the area of the stick diagram:

$$\begin{aligned} A &= WH \\ &= (40\lambda)(48\lambda) \\ &= 1920\lambda^2 \end{aligned}$$

(d)

The layout diagram using CAD tool is shown in Figure 3:



(e)

Now measure the area of layout and compare it to the area estimate from the stick diagram. Recall that λ is just half of the minimum width of a transistor in the process. The actual layout area and its estimate should match or at least be very close. The layout shown in Figure 3 has an area that matches the estimate.

1.19 Design a 3-input minority gate using CMOS NANDs, NORs, and inverters. How many transistors are required? How does this compare to a design from Exercise 1.18(a)?

Consider a three input majority function, and the logic expression is as follows.

$$Y = A(B+C)+BC \quad \ldots\ldots (1)$$

Write the logic expression of the minority function for the equation (1).

$$Y = \overline{A(B+C)+BC} \quad \ldots\ldots (2)$$

The schematic of CMOS logic gates for the logic expression shown in equation (2) is as shown in Figure 1.

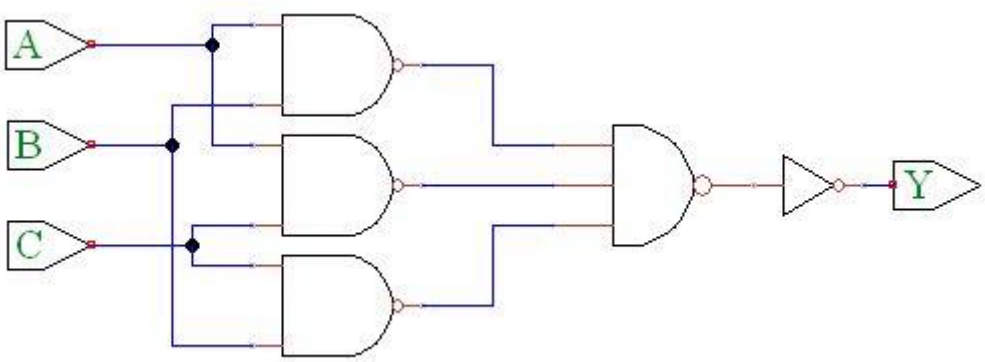


Figure 1: CMOS logic gate level schematic of minority function.

To implement a NAND gate using the transistor level schematic, it is clear that two NMOS transistors are to be connected in series and two PMOS transistors are to be connected in parallel which are placed in series to the NMOS transistors.

,to implement a NOR gate using the transistor level schematic, two NMOS transistors in parallel and two PMOS transistors in series are to be connected in series and should also be placed in series to the two parallel NMOS transistors.

,To implement an inverter one NMOS transistor and PMOS transistor are to be placed in series.

It is clear from the basic concept of transistor level schematic that to implement the Figure 1 using transistor level schematic each two input NAND gate requires 4 gates, three input NAND gate requires 6 transistors and an inverter requires 2 gates.

the total number of gates required to implement the Figure 1 using transistor level schematic.

there exists 3 two input NAND gates and 1 three input NAND gate and an inverter.

There exists 3 two input NAND gates, so the number of transistors required are (3×4), that is 12 transistors are required.

There exists one 3 input NAND gate, so the number of transistors required are 6.

There exists one inverter, so the number of transistors required is 2.

The total number of transistors required to implement the Figure 1 using the transistor level schematic is 20.

the Figure 1.18(a) represents a CMOS compound gate.

the logic expression shown in equation (2) can be implemented using the CMOS compound gate.

Use the basic concepts of designing of the NAND and NOR gates in transistor level schematic and draw the CMOS compound gate for the logic expression shown in equation (2).

Thus, transistor level schematic of minority function shown in equation (2) with single stage of logic is shown in Figure 2.

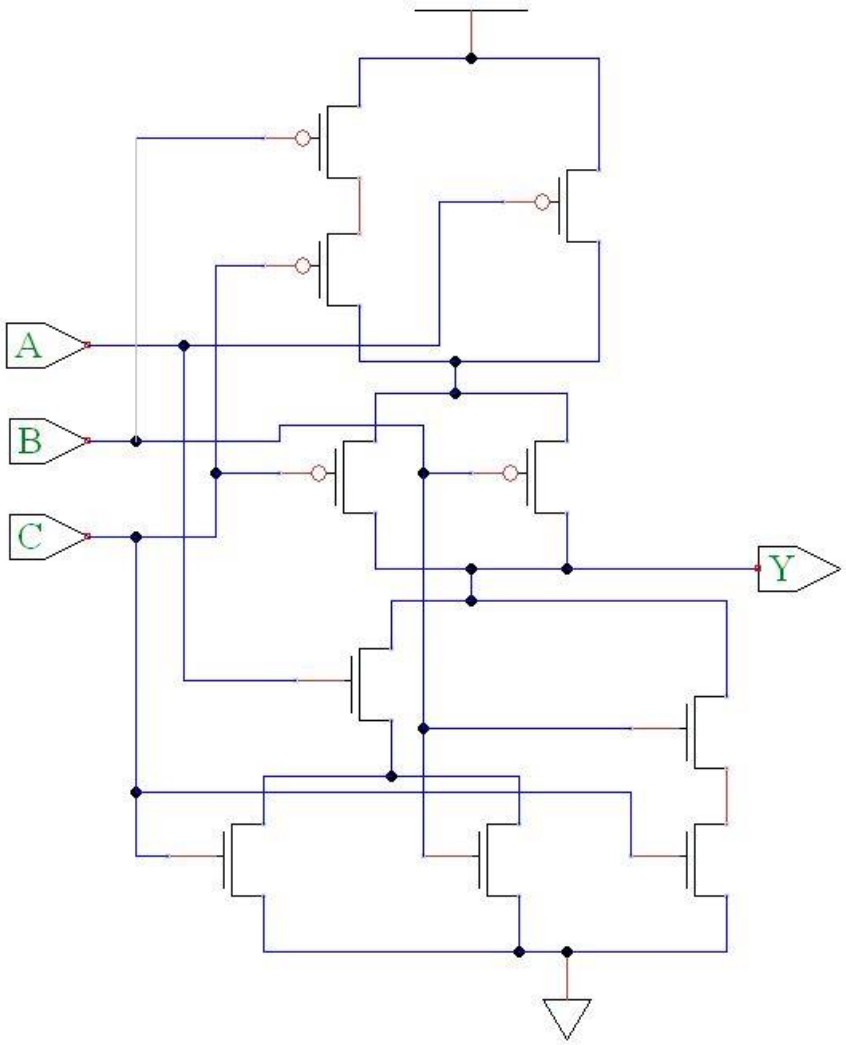


Figure 2

from the Figure 2 that to implement the logic expression of the minority function shown in equation (2), 10 gates are required.

to implement the logic expression shown in Equation (2) using the Figure 1 20 transistors are required and to implement the same logic expression using the CMOS compound gate 10 transistors are required.

Thus, the number of transistors required to implement the logic expression shown in equation (2) using the CMOS compound gate are **less** than the number of the transistors required to implement the CMOS logic gate level schematic shown in Figure 1.

1.20 A carry lookahead adder computes G = G3 + P3(G2 + P2(G1 + P1G0)). Consider designing a compound gate to compute G.
a) sketch a transistor-level schematic
b) sketch a stick diagram
c) estimate the area from the stick diagram

(a)

$$G = G_3 + P_3\left(G_2 + P_2\left(G_1 + P_1G_0\right)\right) \quad \ldots\ldots (1)$$

the logic expression of $\overline{G}$.

$$\overline{G} = \overline{G_3 + P_3\left(G_2 + P_2\left(G_1 + P_1G_0\right)\right)} \quad \ldots\ldots (2)$$

The logical expression of the OR-AND-INVERT gate is shown in equation (3).

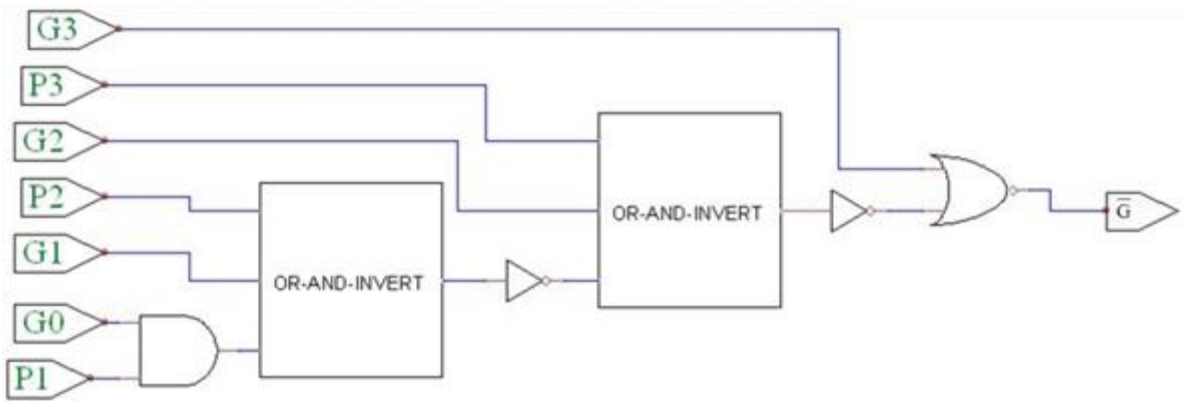
$$Y = \overline{(A+B)\bullet C} \quad \ldots\ldots (3)$$

It is clear from the expression 3 that the equation (2) can be easily implemented using the OR-AND-INVERT gates.

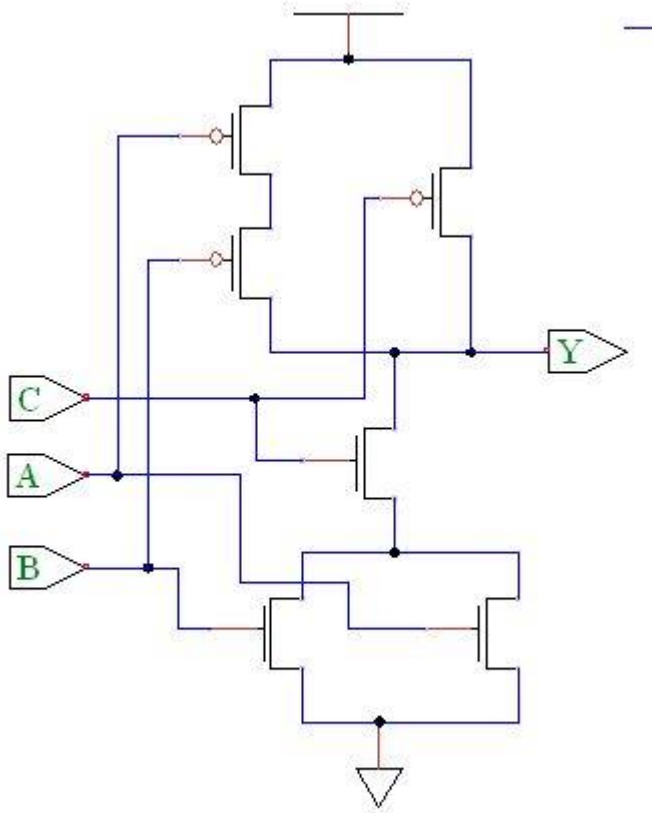
Use an AND gate to obtain the expression P_1G_0 and then use an OR-AND-INVERT gate to implement $\overline{P_2\left(G_1 + P_1G_0\right)}$ and use an inverter to obtain $P_2\left(G_1 + P_1G_0\right)$.

Use second OR-AND-INVERT gate to implement $\overline{P_3\left(G_2 + P_2\left(G_1 + P_1G_0\right)\right)}$ and an inverter to obtain $P_3\left(G_2 + P_2\left(G_1 + P_1G_0\right)\right)$.Then use a NOR gate to implement $\overline{G_3 + P_3\left(G_2 + P_2\left(G_1 + P_1G_0\right)\right)}$.

The gate level schematic using OR-AND-INVERT gates is shown in Figure 1.



Draw the CMOS compound gate for the logic expression of the OR-AND-INVERT logic gate shown in equation (3).



Draw the transistor schematic for the equation (2) using the Figure 2 as shown in the

Figure 3.

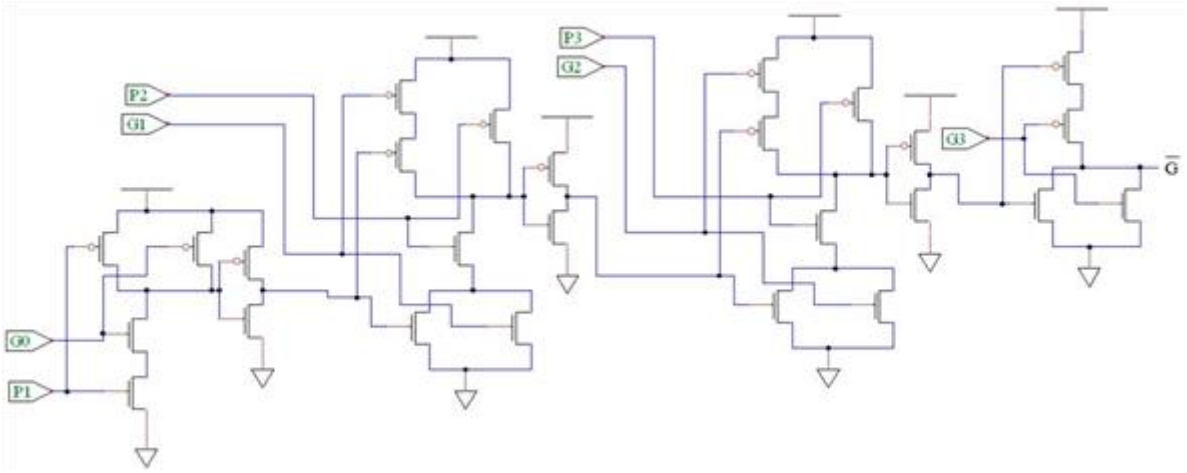


Figure 3: Transistor level schematic of $G = G_3 + P_3\left(G_2 + P_2\left(G_1 + P_1 G_0\right)\right)$.

(b)

Draw the stick diagram for the equation (2) using the Figure 3 as shown in Figure 4.

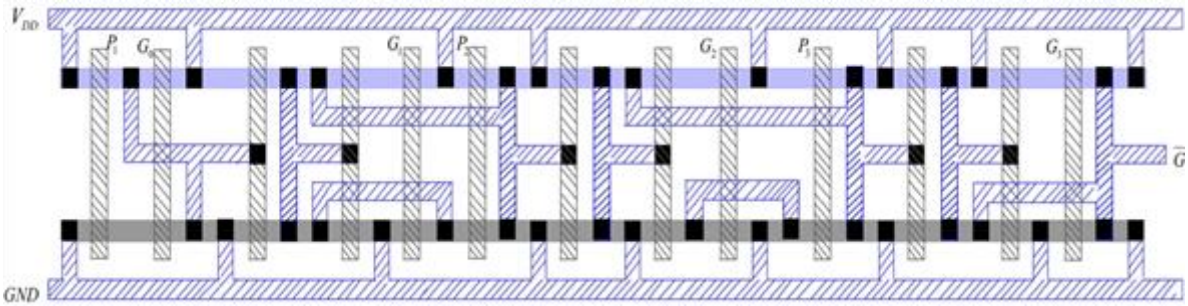
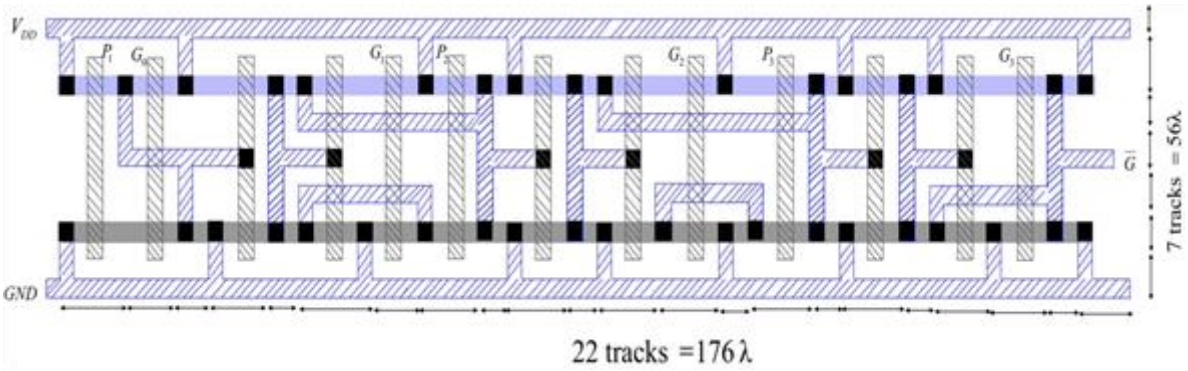


Figure 4: stick diagram of minority function $\overline{G}$

(c)

Obtain the number of vertical and horizontal tracks from the stick diagram as shown in Figure 5.



It is clear from the stick diagram shown in Figure 5 that the vertical tracks are 7 and the horizontal tracks are 22 and each wire is of 4λ wide and needs a spacing of 4λ then the track pitch is 8λ.

Thus, the total horizontal track occupies a breadth of $(7.(8\lambda))$ that is 56λ and the total vertical track occupies a length of $(22.(8\lambda))$ that is 176λ.

Calculate the area from the stick diagram.

$$\text{Area}=56\lambda(176\lambda)$$
$$=9856\lambda^2$$

Thus, the total area of the stick diagram is $\boxed{9856\lambda^2}$.