M R

Ahmed Mahdy

فيزياء	استاتيكا
دوائر كهربية	الكـــترونيات
ميكانيكا الانشائات	هيدروليكا

مدرس خصوصي

اونلاين

حضوري

يحصل الطالب علي

- مقاطع فيديوهات لشرح المقرر بشكل وافي
- ملخص للمادة Pdf للمذكرة والمراجعة
- محاضرات مباشرة علي برنامج زووم
- لمناقشة الأجزاء الغير مفهومة
- تواصل مستمر مع معلم المادة

للتواصل

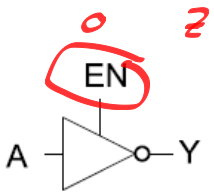
0567630097

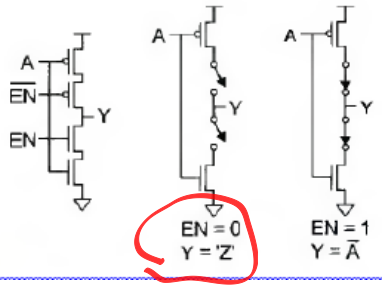
0565657741

Tristates

- *Tristate inverter* produces Z when not enabled

EN	A	Y
0	0	Z
0	1	Z
1	0	1
1	1	0

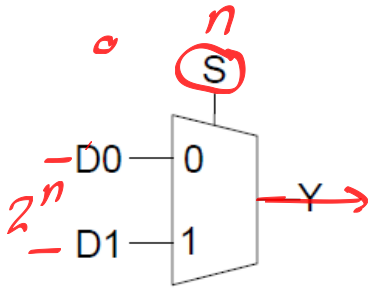




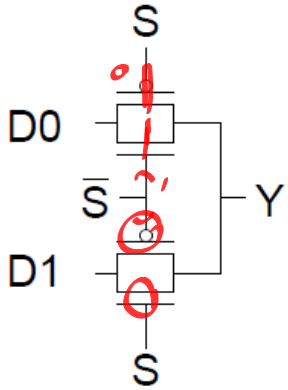
Multiplexers

- 2:1 multiplexer chooses between two inputs

S	D1	D0	Y
0	X	0	0
0	X	1	1
1	0	X	0
1	1	X	1

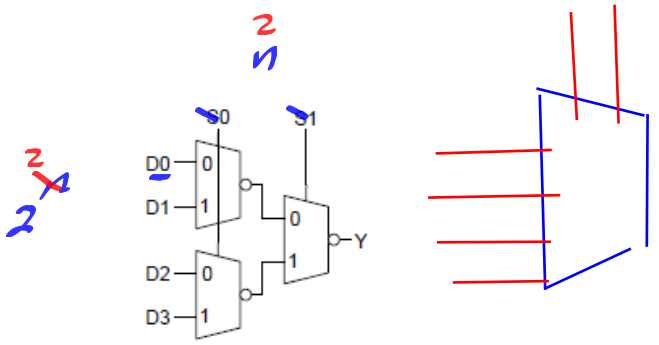


- Nonrestoring mux uses two transmission gates
  - Only 4 transistors



4:1 Multiplexer

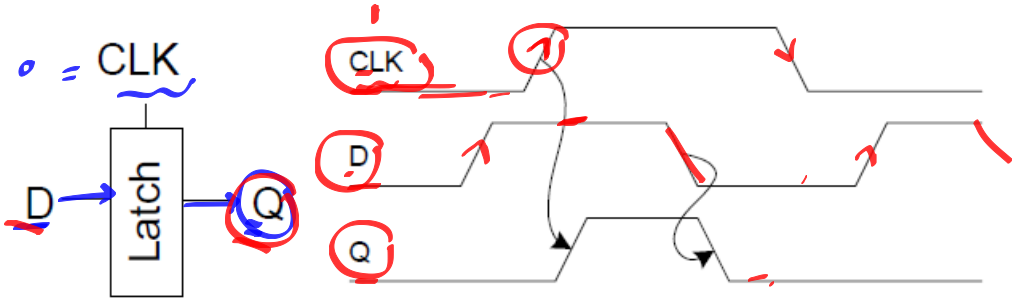
- 4:1 mux chooses one of 4 inputs using two selects
  - Two levels of 2:1 muxes



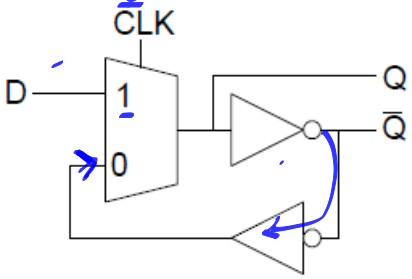
S_0	S_1	
0	0	$D_0 = y$
0	1	$D_1 = y$
1	0	$D_2 = y$
1	1	$D_3 = y$

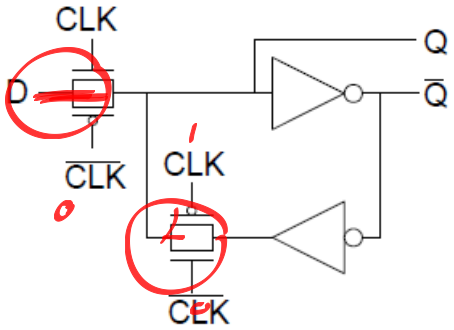
D Latch

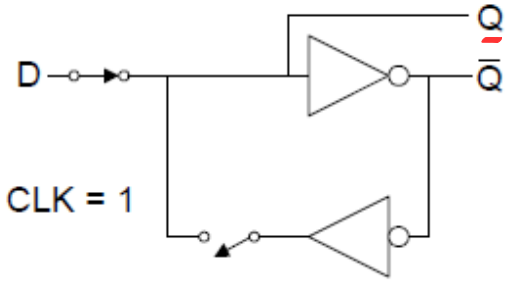
- When CLK = 1, latch is *transparent*
  - D flows through to Q like a buffer
- When CLK = 0, the latch is *opaque*
  - Q holds its old value independent of D
- a.k.a. *transparent latch* or

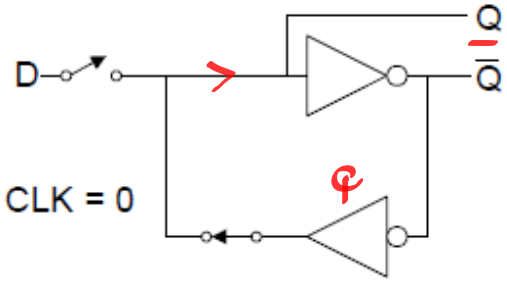


- Multiplexer chooses D or old Q



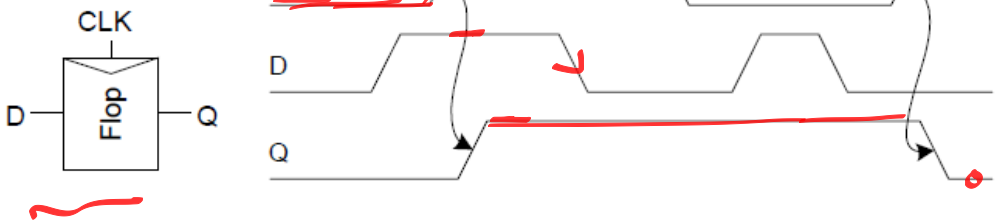






D Flip-flop

- When CLK rises, D is copied to Q
- At all other times, Q holds its value
- a.k.a. *positive edge-triggered flip-flop*, *master-slave flip-flop*



- Built from master and slave D latches