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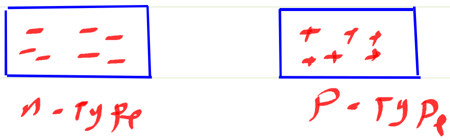
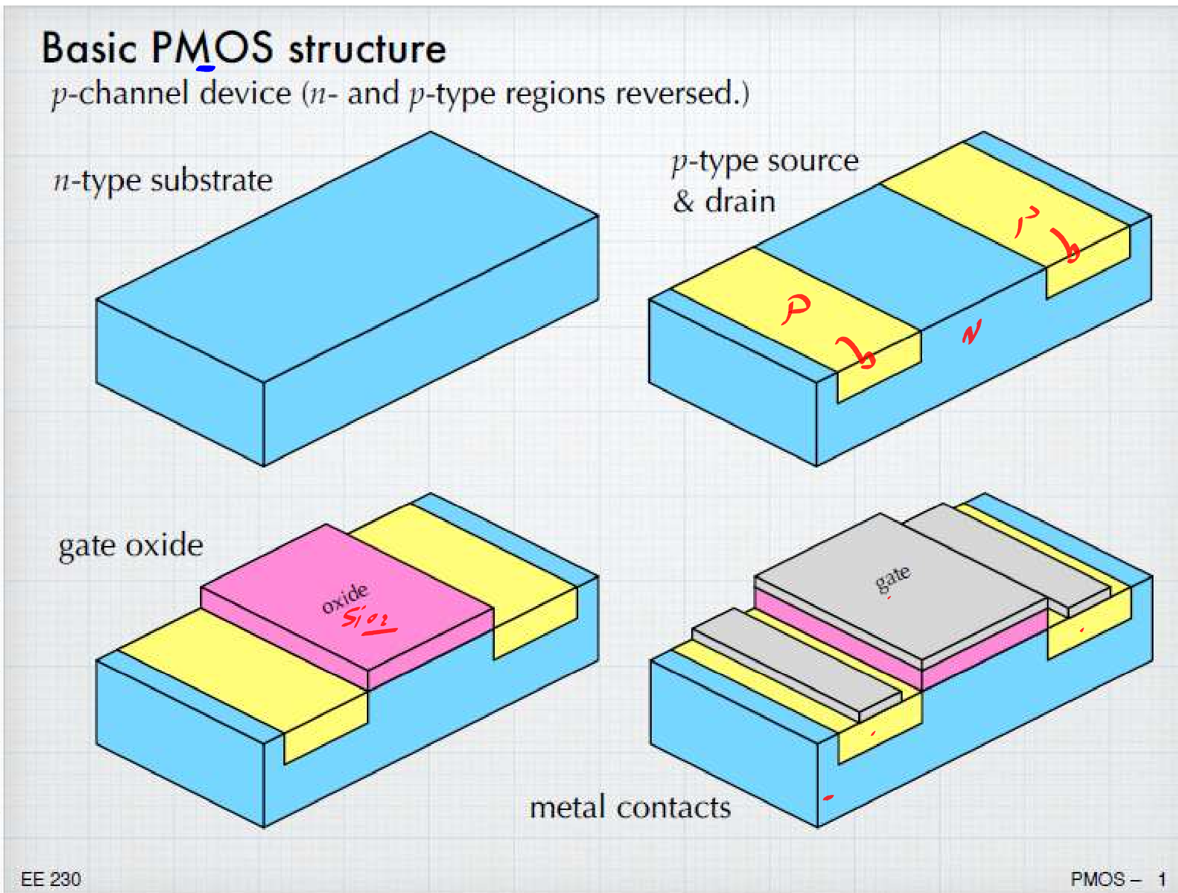
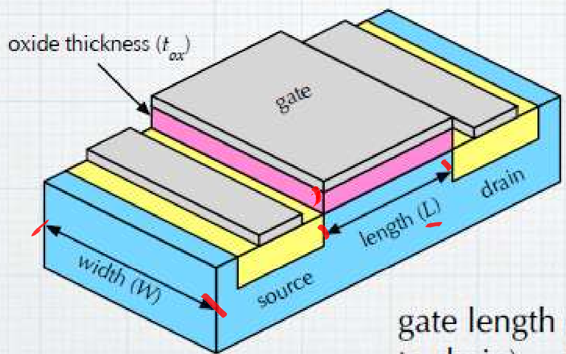

n-type
p-type


Basic PMOS structure
p-channel device (n- and p-type regions reversed.)
n-type substrate
p-type source & drain
gate oxide
oxide
SiO2
gate
metal contacts
EE 230
PMOS – 1

Critical dimensions

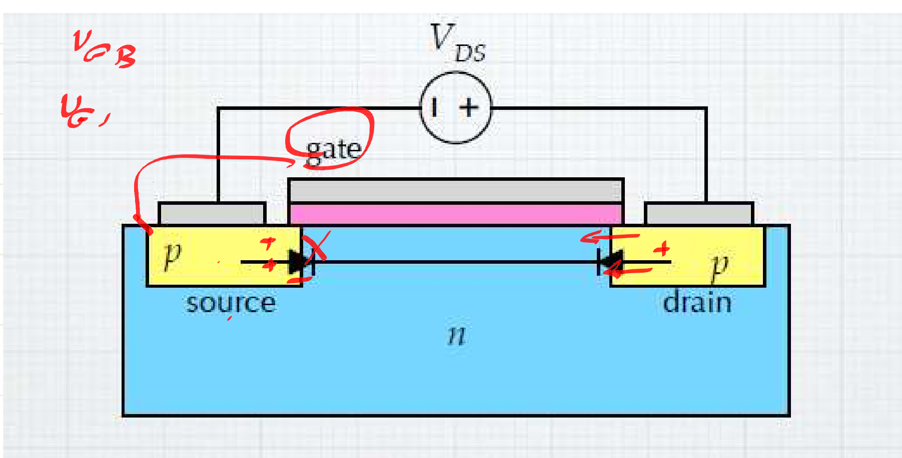
oxide thickness: typical 1 - 10 nm.

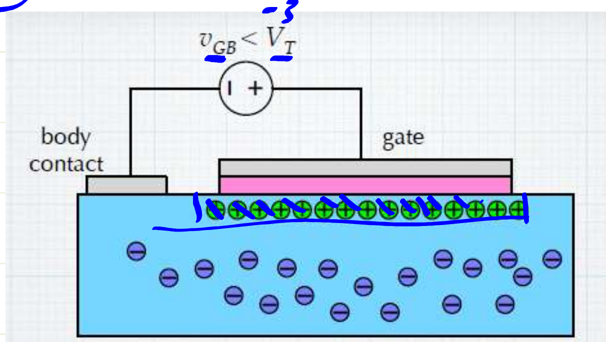


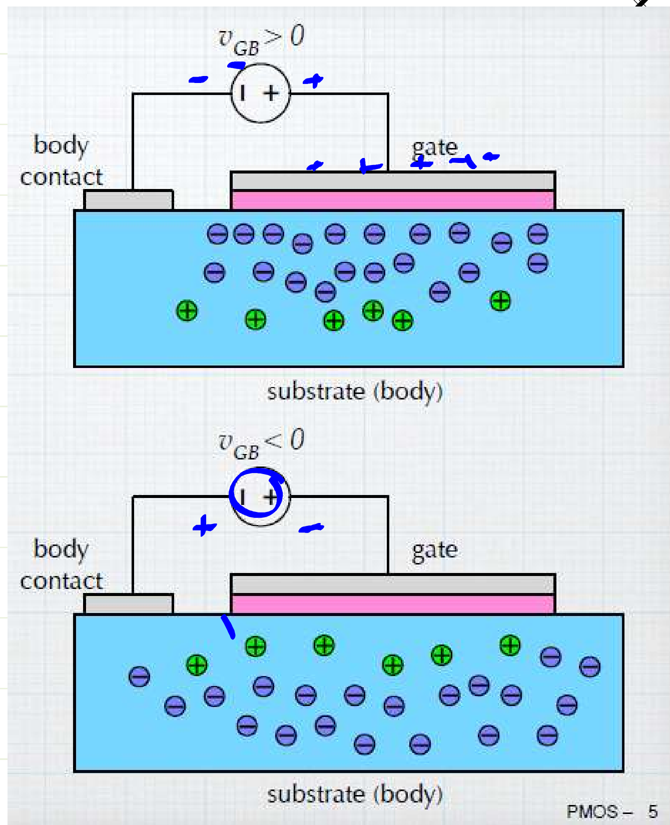
width: typical L to 10 L
(W/L ratio is important)

gate length (distance from source to drain) – currently as small as 20 nm.

EE 230 PMOS – 2

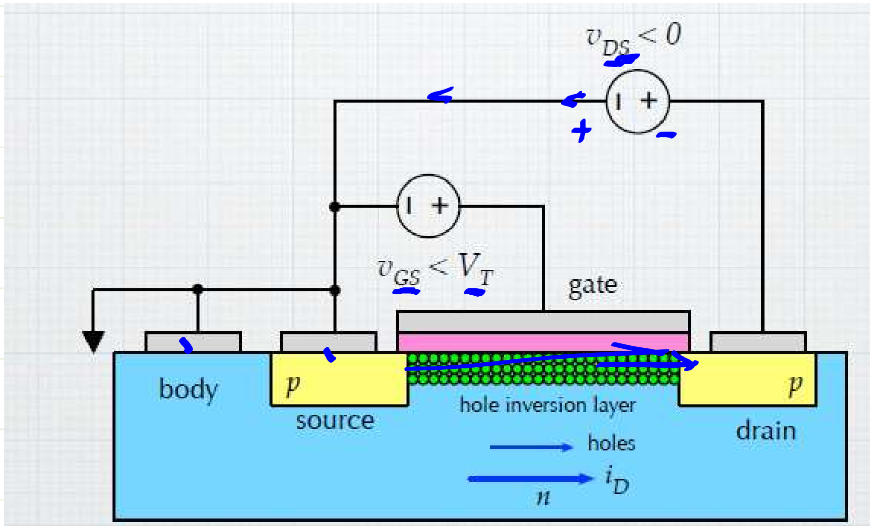






$v_{GB} > 0$	electron accumulation
$V_T < v_{GB} < 0$	carrier depletion
$v_{GB} < V_T$	inversion – hole sheet forms. (Note: V_T is negative.)

$v_{DS} > v_{GS} - v_T$

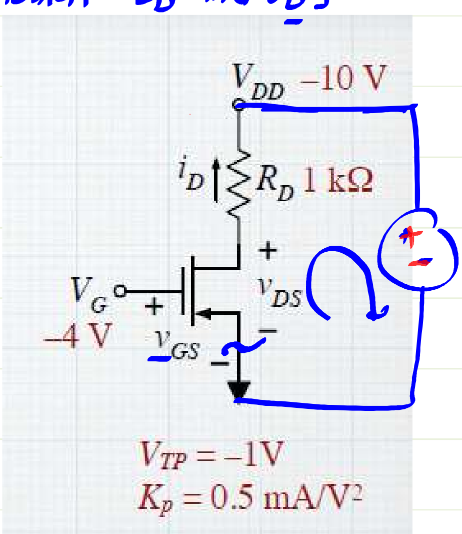


$$i_D = k[2(v_{GS} - v_T)v_{DS} - v_{DS}^2] \quad , \quad v_{DS} > v_{GS} - v_T$$

$$i_D = k[v_{GS} - v_T]^2 \qquad v_{DS} < v_{GS} - v_T$$

PMOS example

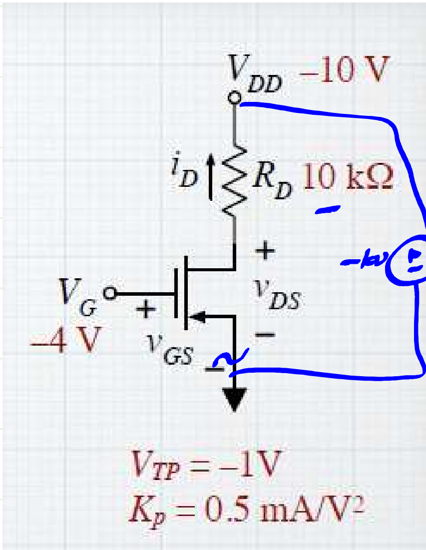
Calculate i_D and v_{DS}



$$i_D = k[v_{GS} - v_T]^2$$
$$= 0.5[-4-(-1)]^2 = 4.5 \text{ mA}$$

$$-v_{DS} + 1\cancel{k} \times 4.5\cancel{m} - 10 = 0$$
$$v_{DS} = -5.5 V$$

$$v_{DS} < v_{GS} - v_T$$
$$-5.5 \qquad -4-(-1)$$
$$-5.5 < -3$$



$$-V_{DS} + i_D \times 10 - 10 = 0$$

$$i_D = \frac{V_{DS} + 10}{10} = \frac{V_{DS}}{10} + 1$$

$$i_D = k[2(V_{GS} - V_T)V_{DS} - V_{DS}^2]$$

$$\frac{V_{DS}}{10} + 1 = 0.5(2(-3)V_{DS} - V_{DS}^2] = -3V_{DS} - 0.5V_{DS}^2$$

$$0.5V_{DS}^2 + \left(\frac{1}{10} + 3\right)V_{DS} + 1 = 0$$

$V_{DS_1} = -0.34V,$	$V_{DS_2} = -5.86V$
$-0.34 > -3$ ✓	$-5.86 \not> -3$

$$i_D = \frac{-0.34}{10} + 1 = 0.966\ mA$$

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Summary of PMOS equations

$v_{GS} > V_T$	$i_D = 0$	off
$v_{GS} < V_T$ $v_{DS} > v_{GS} - V_T$	$i_D = K[2(v_{GS} - V_T)v_{DS} - v_{DS}^2]$	ohmic or linear
$v_{GS} < V_T$ $v_{DS} < v_{GS} - V_T$	$i_D = K[v_{GS} - V_T]^2$	saturation