



مدرس خصوصى



اونلاين

يحصل الطالب على ...

***مقاطع فيديو هات لشرح المقرر بشكل وافي**

***ملخص للمادة للمراجعة النهائية**

***محاضرات مباشرة على برنامج Zoom**

***تواصل مستمر مع معلم المادة للمناقشة**

للتواصل



00201024041097



00201096019763

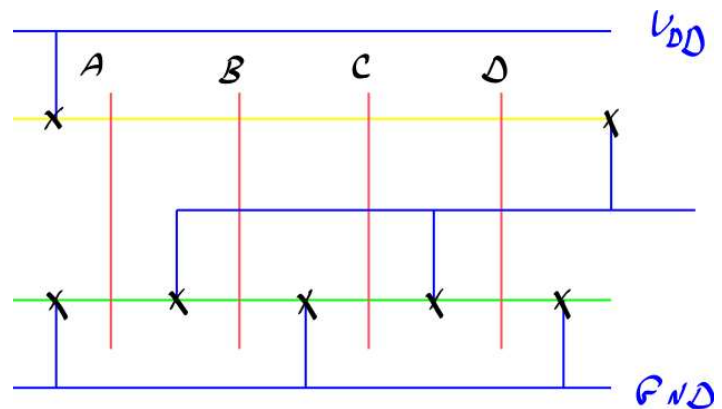
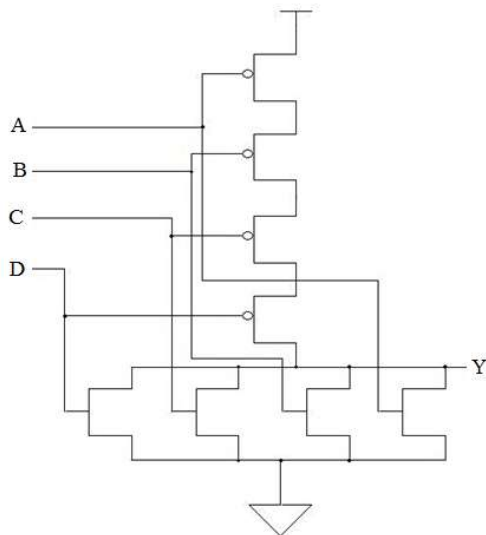
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Sketch a transistor-level schematic for a CMOS 4-input NOR gate and sketch the corresponding stick diagram.

the truth table for a 4-input NOR gate.

W	X	Y	Z	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Observe from the truth table that the output is high when all of the input are low and that the output is low when at least one of the inputs is high. This means that in the transistor schematic, the PMOS transistors must be in series and the NMOS transistors must be in



Observe from the schematic that when all of the inputs are low the 4 NMOS transistors are turned off so there is connection between the output and ground. The 4 PMOS transistors on the other hand will all be on so the output will get pulled up to V_{DD} . If one of the inputs is high then the output cannot get pulled up to V_{DD} ; instead one of the NMOS transistors will be turned on and the output will be pulled down to ground. Therefore this schematic acts exactly like a 4 input NOR gate.

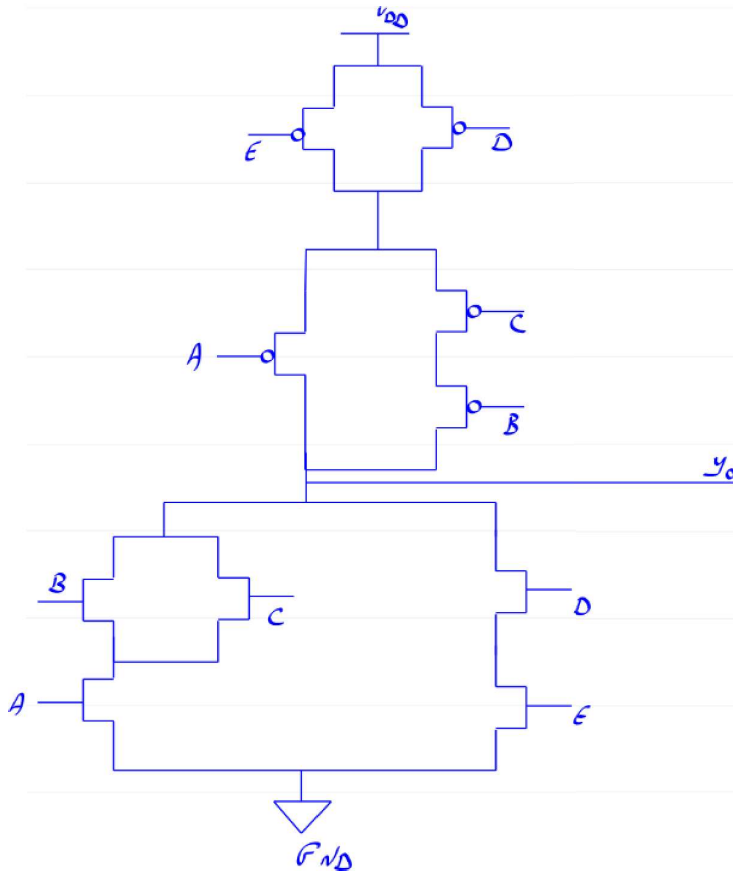
2. Sketch a transistor-level schematic for a compound CMOS logic gate for each of the following logic functions:

a. $Y = \overline{A(B+C) + DE}$

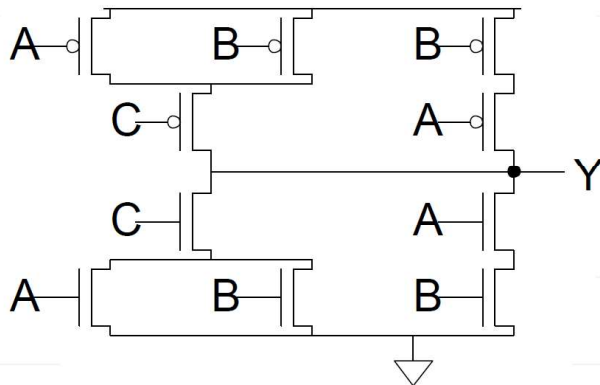
b. $Y = \overline{AB + C \cdot (A+B)}$

c. $Y = \overline{ABC + D}$

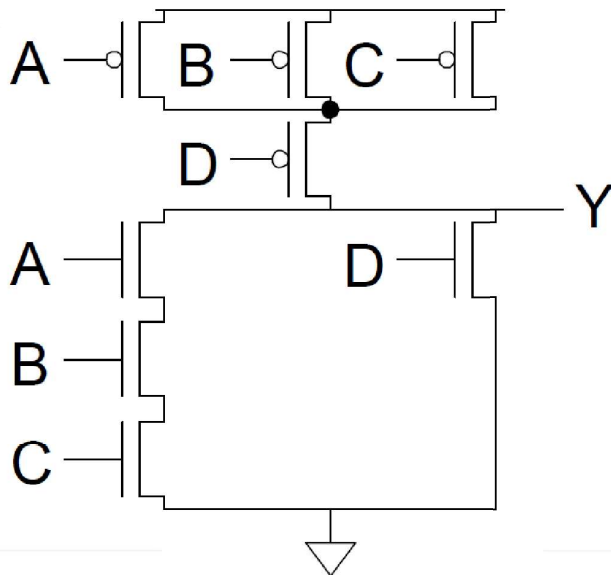
a.



b.



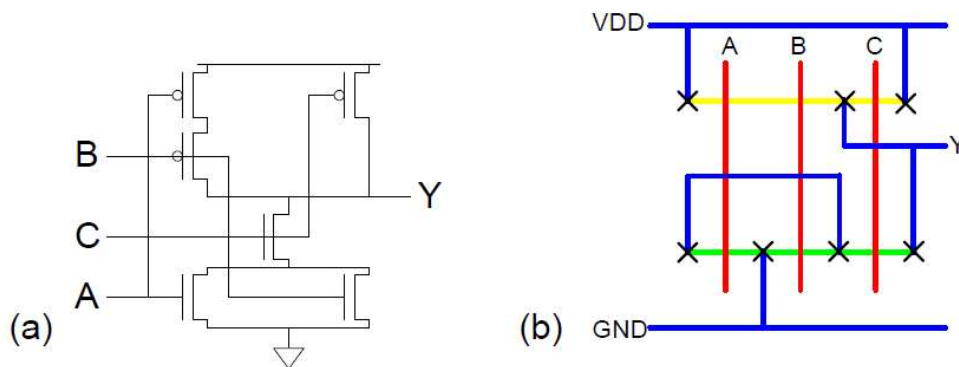
c.



3. Consider the design of a CMOS compound OR-AND-INVERT (OAI21) gate

Computing $F = ((A + B) \cdot C)'$

- sketch a transistor-level schematic
- sketch a stick diagram
- estimate the area from the stick diagram

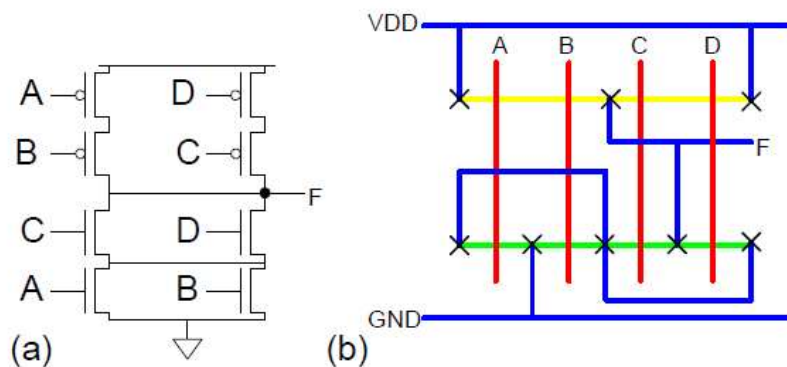


(c) 4×6 tracks = $32 \lambda \times 48 \lambda = 1536 \lambda^2$.

4. Consider the design of a CMOS compound OR-OR-AND-INVERT (OAI22) gate computing $F = ((A + B) \cdot (C + D))'$

gate computing $F = ((A + B) \cdot (C + D))'$

- sketch a transistor-level schematic
- sketch a stick diagram
- estimate the area from the stick diagram



(c) 5×6 tracks = $40 \lambda \times 48 \lambda = 1920 \lambda^2$. (with a bit of care)