Logic Simulation of Sequential circuits in DSCH

4

WEEK

SKILL MATRIX

LEARNING OUTCOMES

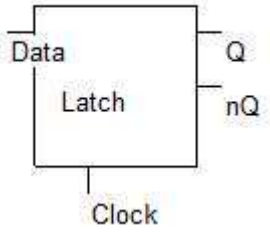
Please define the learning outcomes here

1- D-Latch
2- D-Flip-flop

D-Latch:

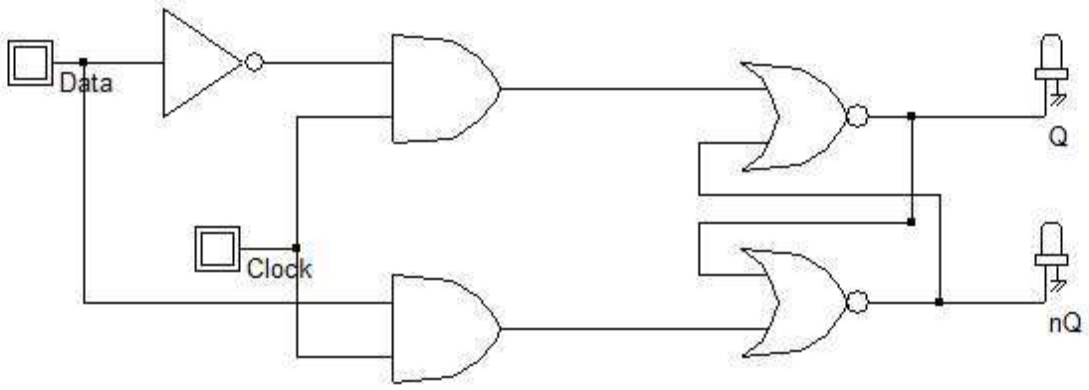
In D-latch is controlled by a clock .when the clock input is high, the latch output ***Q*** follows the change of the input ***D***. The latch is transparent .Now when the clock input goes low; the latch is in memory mode, meaning that it produces the value stored in the loop at the output ***Q***. The latch holds the memory state as long as the two inverters are supplied.

Latch Symbol :



D	Clock	Q	nQ
0	0	Q	nQ
0	1	0	1
1	0	Q	nQ
1	1	1	0

Schematic of D-latch:



When performing the logic simulation ***Q*** and ***nQ*** starts with an undetermined state. Once the clock is active ***Q*** and ***nQ*** turn to a deterministic state, as the data input ***D*** is transferred to ***Q***, and its opposite to ***nQ***. When clock returns to level ***0***, the latch keeps its last value.

Simulate the schematic and verify the truth table and draw the timing diagram .

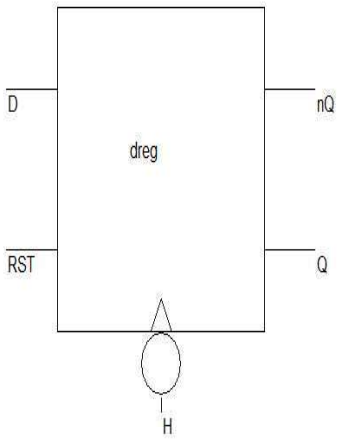
Timing Diagram:

D Flip-Flop :

The main limitation of the D latch is its inadequacy to build shift registers or counters. On a positive level of the clock , the whole series of D latches is transparent to the input data.

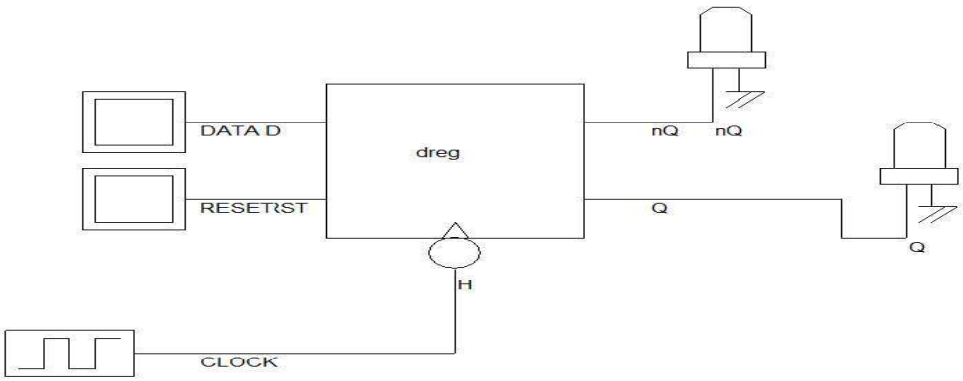
In order to overcome the limitation of latches when trying to build registers, we use edge-triggered latches, wherein the information flows from the input D to the output Q only at a rise edge of the clock. The latch is commonly known as D-Flip Flop(DFF).

Symbol of DFF:

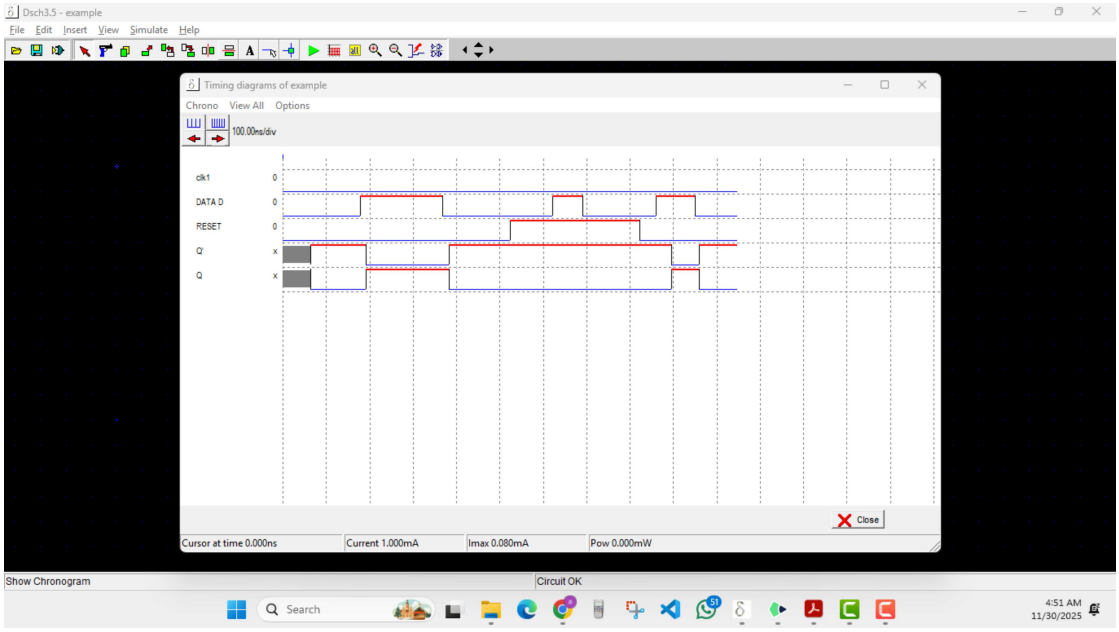


Notice that the triangle at the clock input recalls the sensitivity of outputs Q and nQ to the edge of the clock. The circle indicates that this Dreg cell is sensitive to a fall edge of the clock.

Schematic of D-flip flop:



Timing Diagram of D-flipflop:



Observation:

Write the difference between the d-latch and d-flip flop timing diagram.

In D-latch is controlled by a clock .when the clock input is high, the latch output Q follows the change of the input D. The latch is transparent .Now when the clock input goes low; the latch is in memory mode, meaning that it produces the value stored in the loop at the output Q

in D-flip-flop the information flows from the input D to the output Q only at a rise edge or fall edge of the clock.